EE/CprE/SE 4920 WEEKLY REPORT 2

Digital ASIC Fabrication

10/31/24 - 11/14/24

Group Number: SDDec24-12

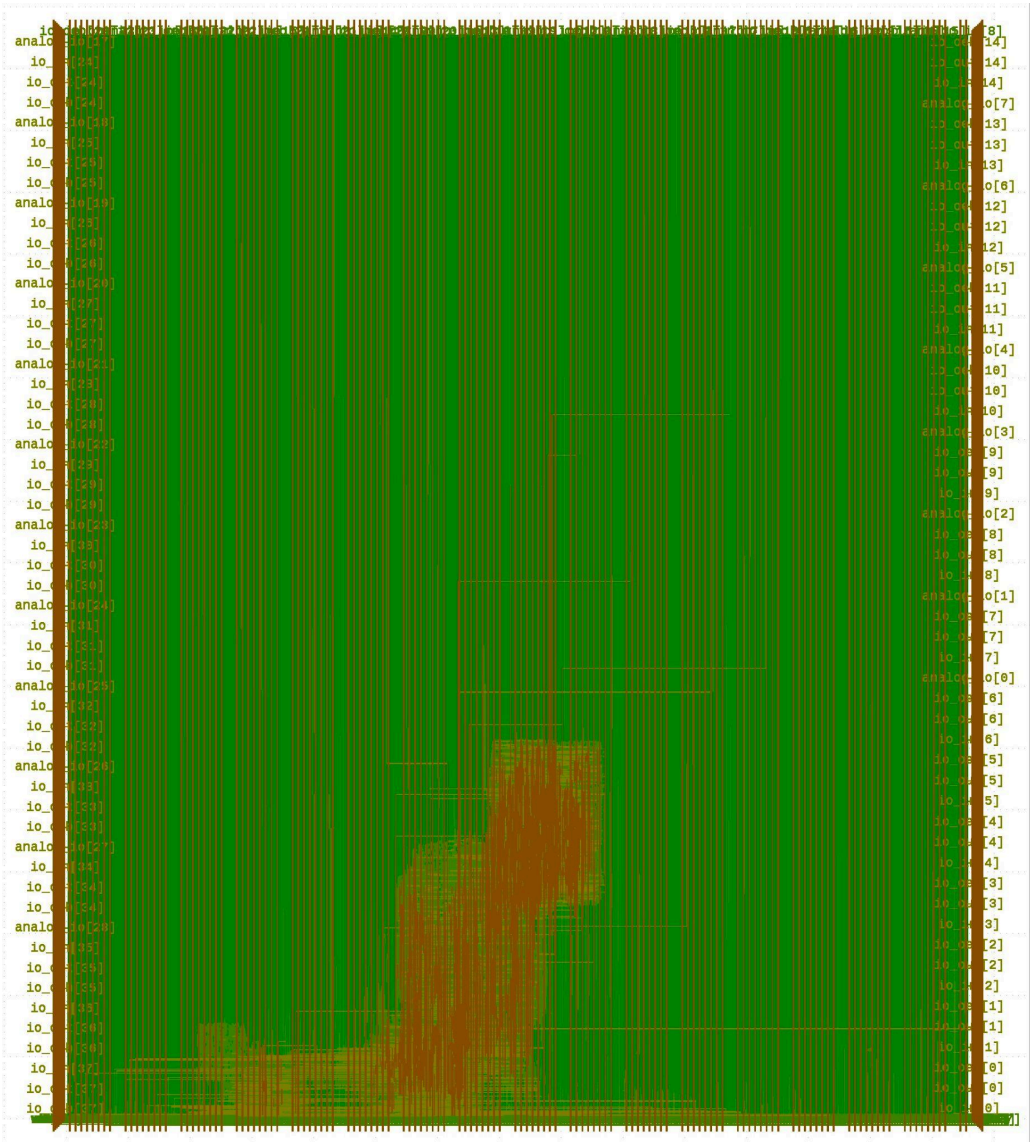
Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

Tapeout deadline was Monday, November 11!

Final Hardened Design:



Past Week Accomplishments

- **Mitchell:** Helped with integrating our final set of projects into the framework we designed. This included a total of 8 projects that could individually be selected and used within our framework. I also helped with writing/testing our design using C code. This process did require communication with the designer of the project creators as the projects we are using within our framework are not our responsibility but collaboration is required to ensure everything works properly and that we have a successful tapeout.
- **Evan:** Ran a precheck to ensure functionality, worked with Gregory to perform bug fixing on core functionality. Assisted with C code testing (again with Gregory as a guiding influence).
- **Baoshan:** Do research about how to test the bless board and design the bring up plan for the project test.
- **Katie:** Reworked entire framework logic to simplify our design. Wrote and ran RTL and GL simulations with C code. Tested two different projects on the FPGA and verified they functioned correctly. Ran multiple iterations of hardening and precheck with different student projects. Worked with Gregory to finalize the student projects going into our framework and resolve timing violations. Submitted our design for tapeout and talked with Efabless about our submission.

Pending Issues

- **Mitchell:** We had some timing issues that required us to meet with the Efabless team to discuss whether they were critical errors and how to fix them.
- **Evan:**Timing issues that may be resolved by decreasing the MAX_FANOUT constant in the config.
- **Baoshan:**
- **Katie:** Timing issues?

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Helped integrate the final set of projects into our framework. Helped with writing and testing C code on our final design.	10	70
Evan		9	N/A
Baoshan	Test and start the Efabless development board to ensure stable operation of the project	5	45
Katie	Wrote C code tests, ran RTL and GL simulations and tests on the FPGA, ran hardening, precheck, and full-chip STA on our final design	20	70

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Begin updating our final design document, considering poster ideas, and thinking about our final presentation.	Everyone	11/28/24

Advisor Meeting Summary

Meet with Efabless Group during our advisor meeting to discuss timing issues and final submission for tapeout.