EE/CprE/SE 4920 WEEKLY REPORT 2

Digital ASIC Fabrication

10/3/24 - 10-31-24

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

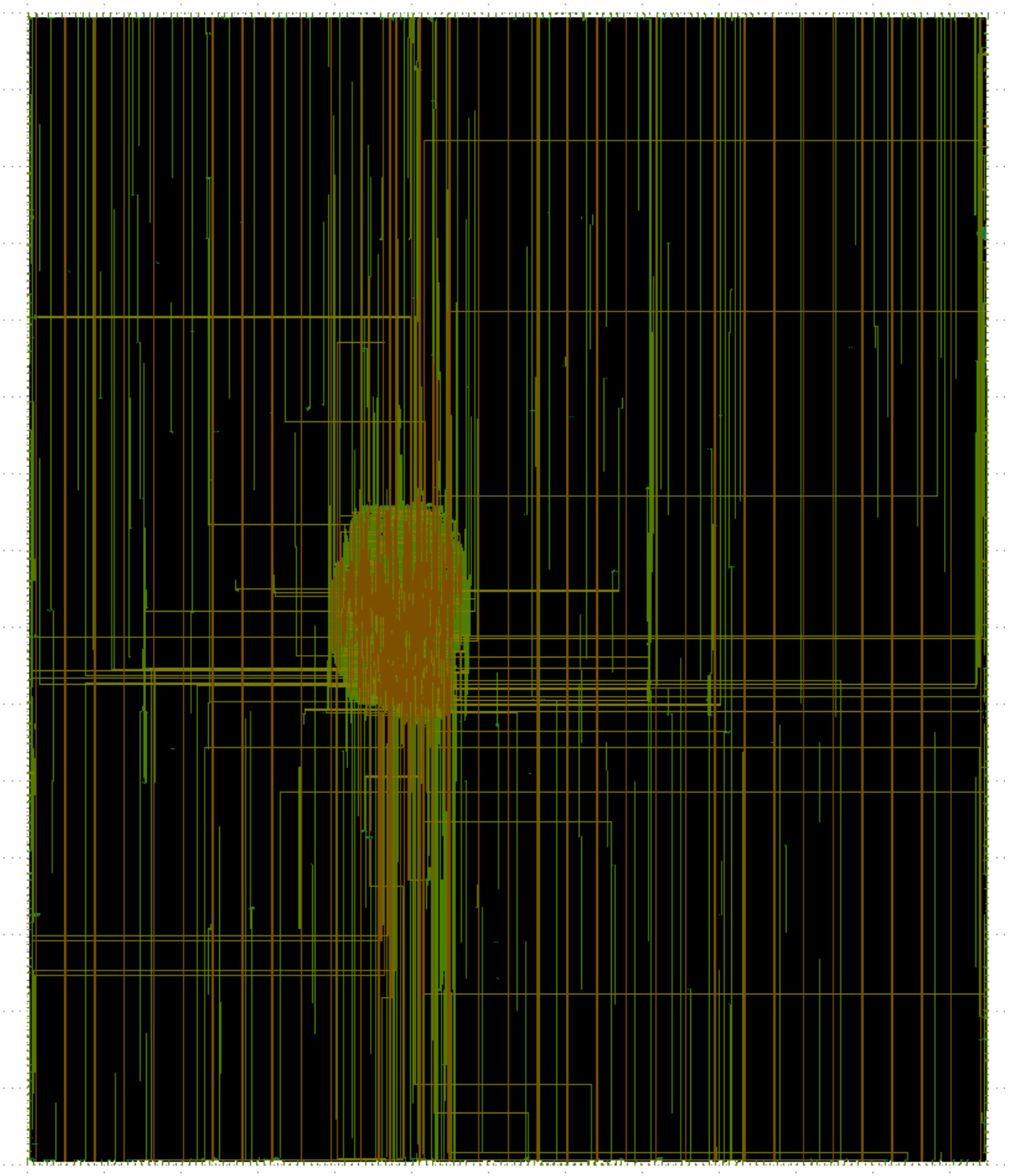
Summary

linter.log

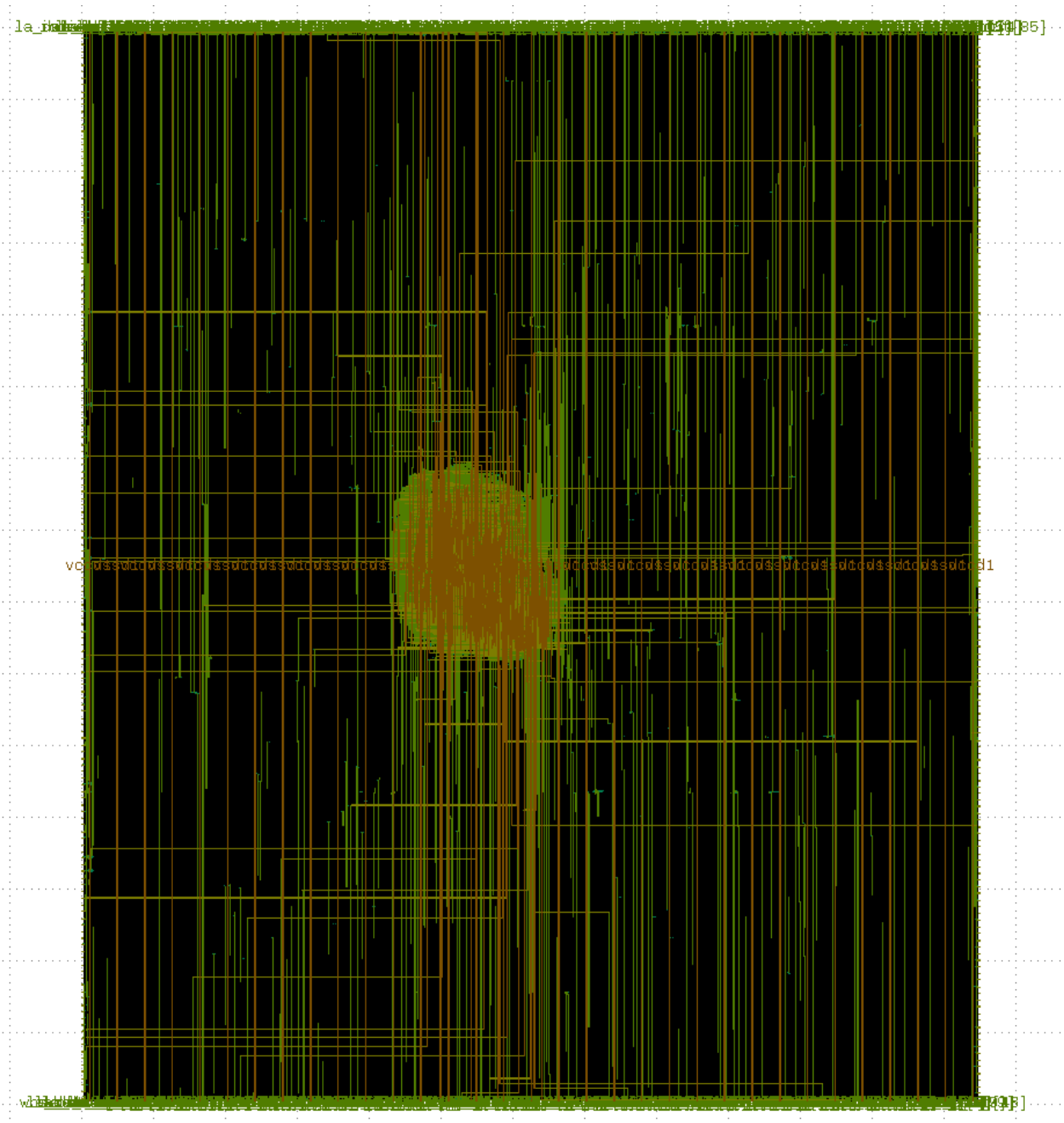
```
%Warning-PINMISSING: /home/mdd1/Desktop/SeniorDesign/sddec24-12/openlane/user_project_wrapper/../../verilog/rtl/
user_project_wrapper.v:117:1: Cell has missing pin: 'vccd1'
  117 | g_proj_final (
      | ^~~~~~~~~~~
                     ... For warning description see https://verilator.org/warn/PINMISSING?v=5.009
                     ... Use "/* verilator lint_off PINMISSING */" and lint_on around source to disable this message.
%Warning-PINMISSING: /home/mdd1/Desktop/SeniorDesign/sddec24-12/openlane/user_project_wrapper/../../verilog/rtl/
user_project_wrapper.v:117:1: Cell has missing pin: 'vssd1'
  117 | g_proj_final (
      | ^~~~~~~~~~~
%Error: /home/mdd1/Desktop/SeniorDesign/sddec24-12/openlane/user_project_wrapper/../../verilog/gl/user_framework.v:1233:27: Can't
resolve module reference: 'sky130_fd_sc_hd__diode_2'
 1233 |  sky130_fd_sc_hd__diode_2 ANTENNA_1 (.DIODE(net1),
      |                           ^~~~~~~~
%Error: Exiting due to 1 error(s)
```

```
1232
1233    sky130_fd_sc_hd__diode_2 ANTENNA_1 (.DIODE(net1),
1234       .VGND(vssd1),
1235       .VNB(vssd1),
1236       .VPB(vccd1),
1237       .VPWR(vccd1));
1238    sky130_fd_sc_hd__diode_2 ANTENNA_10 (.DIODE(net1),
1239       .VGND(vssd1),
1240       .VNB(vssd1),
1241       .VPB(vccd1),
1242       .VPWR(vccd1));
1243    sky130_fd_sc_hd__diode_2 ANTENNA_100 (.DIODE(net6),
1244       .VGND(vssd1),
1245       .VNB(vssd1),
1246       .VPB(vccd1),
1247       .VPWR(vccd1));
1248    sky130_fd_sc_hd__diode_2 ANTENNA_1000 (.DIODE(net9),
1249       .VGND(vssd1),
1250       .VNB(vssd1),
1251       .VPB(vccd1),
1252       .VPWR(vccd1));
1253    sky130_fd_sc_hd__diode_2 ANTENNA_1001 (.DIODE(net9),
1254       .VGND(vssd1),
1255       .VNB(vssd1),
1256       .VPB(vccd1),
1257       .VPWR(vccd1));
1258    sky130_fd_sc_hd__diode_2 ANTENNA_1002 (.DIODE(net9),
1259       .VGND(vssd1),
1260       .VNB(vssd1),
1261       .VPB(vccd1),
1262       .VPWR(vccd1));
1263    sky130_fd_sc_hd__diode_2 ANTENNA_1003 (.DIODE(net9),
1264       .VGND(vssd1),
1265       .VNB(vssd1),
1266       .VPB(vccd1),
```

EE/CprE/SE 4920 WEEKLY REPORT 2



EE/CprE/SE 4920 WEEKLY REPORT 2



EE/CprE/SE 4920 WEEKLY REPORT 2

Past Week Accomplishments

- **Mitchell:** Successfully hardened framework with all modules and one project. Hardened wrapper with all modules and no project. I ran a pre-check on the hardened version of the wrapper, which failed because of LVS. I proceeded to fix the LVS issue and have a version of our wrapper that passes precheck.
- **Evan:** Established functionality by hardening several configurations of the framework. Worked on C test code for the FPGA.
- **Baoshan:** Debug and optimize the connections of GPIO control and Wishbone interface, check their functionality before and after hardening to make sure it is not affected.
- **Katie:** Worked with Mitchell and Evan so that we were all able to harden the wrapper. Successfully hardened and ran precheck on the wrapper and with various combination of projects.

Pending Issues

- **Mitchell:** Writing test code to further confirm the functionality of our code and test all cases that could break the framework.
- **Evan:** finish integrating the c test code but addressing is proving problematic.
- **Baoshan:** LVS does not match. I don't know if there is a problem with DRC or line layout.
- **Katie:** Figure out how to help automate the hardening/precheck process to save time

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Hardened and passed precheck with a version of the final project and continued to work on testing.	10	60
Evan	C programming preliminary steps and a couple hardening passes.	7	49
Baoshan	Hardening framework and ports	5	40
Katie	Hardening and running precheck, debugging issues	8	50

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Keep working on testing.	Mitchell	11/11/24
Work on testing and integrating more projects	Katie	11/11/24
Finish c code.	Evan	11/11/24

Advisor Meeting Summary

- prioritize getting the framework through all tape out checks
- for next week, record all the critical steps to get a design that passes precheck
- set up a way to test everything with C either on the FPGA or in simulation
- create a framework to run a series of tests for all existing projects
    - so when a new project is added, we can run the framework to check all the already existing tests and verify the new project didn't break something
    - regression testing
- start out with basic tests for each project
    - once those are working, then focus on writing more detailed tests, adding more student projects, refactoring jake/gregory's senior design