EE/CprE/SE 4920 WEEKLY REPORT 1

# Digital ASIC Fabrication

08-28-24 – 09-04-24

**Group Number:** SDDec24-12

**Faculty Advisor & Client:** Henry Duwe

**Team Members:** Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

## Summary

During week one of the Fall semester, we met with Duwe on Wednesday to discuss our progress from the previous semester of senior design. This included where each member left off and the future plans for the project. We began integrating each module/component we designed in the previous semester into the project wrapper and continued with the hardening of the User Project Wrapper. We also have been working to harden the OpenRAM wishbone interface individually, and now we are working to integrate that into the User project wrapper. Finally, we set a time to meet every Thursday to work as a group and ensure we are not overlapping work.

## Past Week Accomplishments

- **Mitchell:** I began the integration of submodules into the user project wrapper and began making connections within the wrapper. Wrote the verilog for 32to1mux.
- **Evan:** Established a working openRAM base from the tutorial, however I've run into issues porting this to another top level user_project_wrapper. I will perhaps start over, building an openRAM project from the ground up-eliminating this issue.
- **Baoshan:**
- **Katie:** Successfully hardened OpenRAM in tutorial user_project_wrapper. Started writing Verilog for the OpenRAM wishbone interface. Attempted to harden OpenRAM in our user_project_wrapper but faced errors

## Pending Issues

- **Mitchell:** Didn't write the test bench for the 32to1mux, and have not confirmed that submodules are integrated correctly or if connections are correct.
- **Evan:** As mentioned, *I* am having issues making using openRAM. I will address this in the coming week.
- **Baoshan:**
- **Katie:** Posted the hardening error in Teams for Jake to look at

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## Individual Contributions

| Name | Contributions | Weekly Hrs | Total Hrs |
|---|---|---|---|
| Mitchell | Began integration of sub-modules into user project wrapper, wrote verilog code for 32to1mux | 3 | 3 |
| Evan | Working with openRAM and various top level modules. | | |
| Baoshan | | | |
| Katie | Hardened OpenRAM | 4 | |

## Plans for the Upcoming Week

| Action Item | Person in Charge | Expected Date |
|---|---|---|
| Write testbench for 32to1mux, continue integrating components and making connections within the User Proect Wrapper | Mitchell | 9/11/24 |
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## Advisor Meeting Summary

- The deposit has been paid for the November 11th deadline; this gives us access to tech support from ebfabless/caravel.
- Jake - recommended pushing it further, pushing the task of two simple adder projects through pre-check;
- Don't want to spend too much time on OpenRAM and fail to finish… two options for the future of OpenRAM are to set a deadline and, if not met by then, go to tech support, rapidly go through the rest of the design, and get through pre-check
- Can I write to individual components and continue to build off that… Dont need to be thorough but should be able to show that the modules are working.
- Take tests and be more aggressive, testing edge cases, weird combinations, → trying to break components to ensure we get full coverage.
- Pre-harden example adder from the tutorial and drop that into user project example
- Component testing should be done in C