Digital ASIC Fabrication

IRP Presentation

sddec24-12
Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Client & Faculty Advisor
Dr. Henry Duwe

sddec24-12.sd.ece.iastate.edu

Project Overview

Context

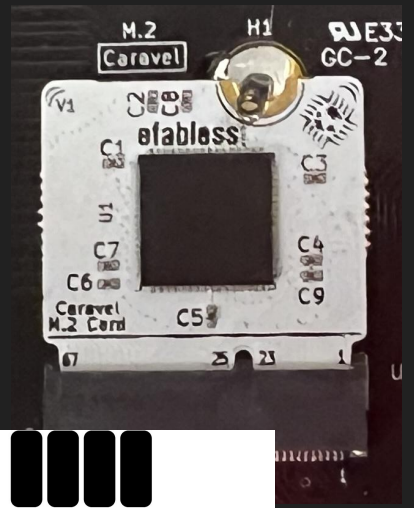
- Undergraduate students rarely design, fabricate, and bring-up custom ASICs

Goal

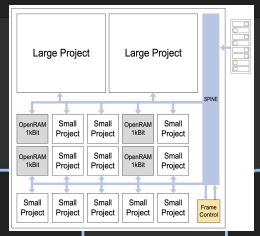
- Support co-curricular at ISU for students interested in chip fabrication

Purpose

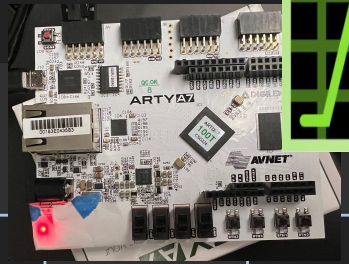
- Chip framework for student projects
- Amortize cost of fabrication

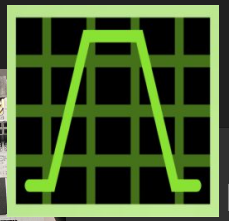


ASIC Design Flow Background




```
always @(*)
begin
    case (wbs_adr_i & 'h0000000F)
        'h0: wbs_dat_ctrl = proj_select;
        'h4: wbs_dat_ctrl = proj_reset;
       default: wbs_dat_ctrl = 'h00000000;
    endcase
end
```

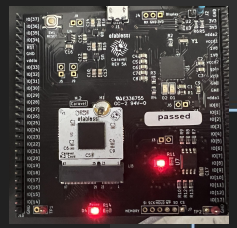


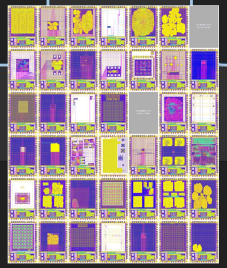


[1]

Chip Design Specification → RTL Design → Functional Verification → Synthesis → Hardening → Sign-off and Verification → Tapeout and Fabrication → Bringup

```
wire _09019_;
wire _09020_;
wire _09021_;
wire _09022_;
wire _09023_;
wire _09024_;
wire _09025_;
wire _09026_;
wire _09027_;
wire _09028_;
wire _09029_;
wire _09030_;
wire _09031_;
wire _09032_;
wire _09033_;
wire _09034_;
wire _09035_;
wire _09036_;
wire _09037_;
```





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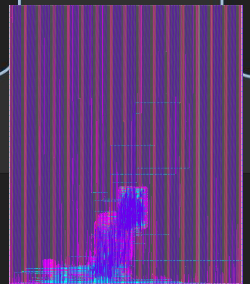

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Users

1.

Future Students

Fabrication opportunities

2.

Professors & Educators

Provide learning opportunities

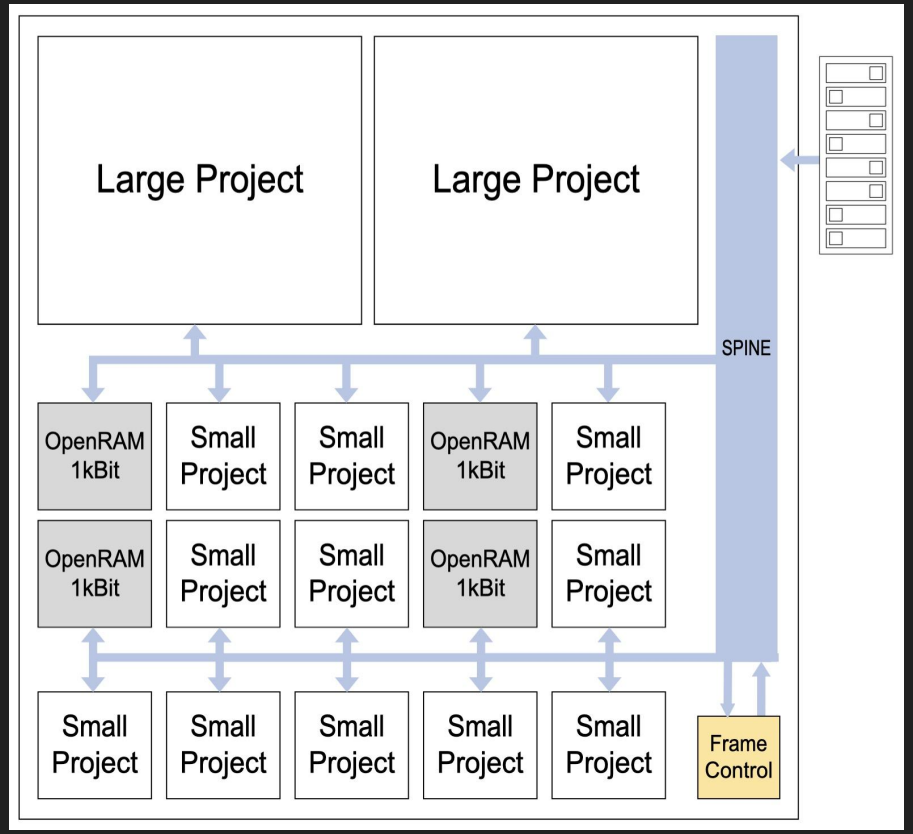
3.

Open-Source Community

Project resources and collaboration

Functional Requirements

- Supports up to 15 total projects
- Software on microcontroller selects which project is active
- One project is active at a time
- Projects interface with Wishbone bus, LA pins, and IO pins
- Design successfully passes precheck and tapeout



Non-Functional Requirements

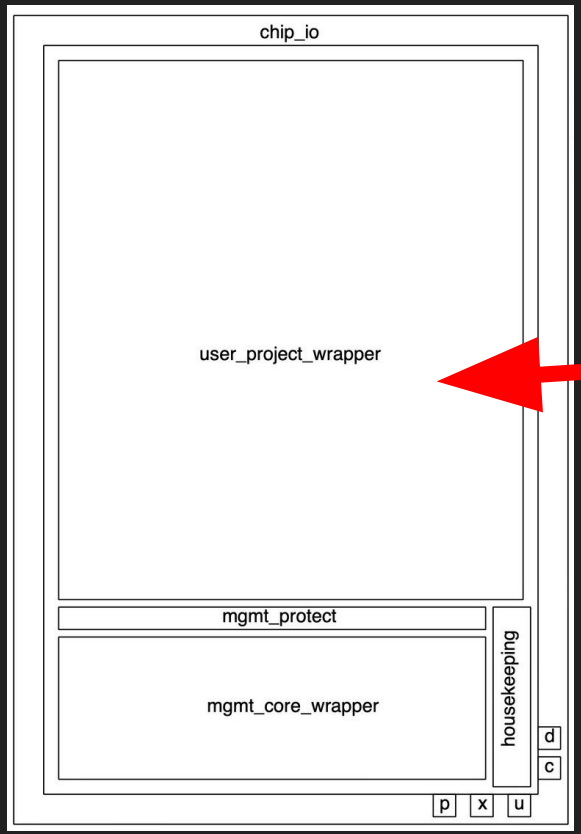
Technical Requirements

- Use Efabless process
- Design implemented in Verilog
- Test code written in Verilog and C
- Frequency of 20 MHz

User-Based Requirements

- Full documentation and bring-up plan
- Straightforward to use with minimal help or troubleshooting
- System is modular and users can expand upon it

High-Level Design



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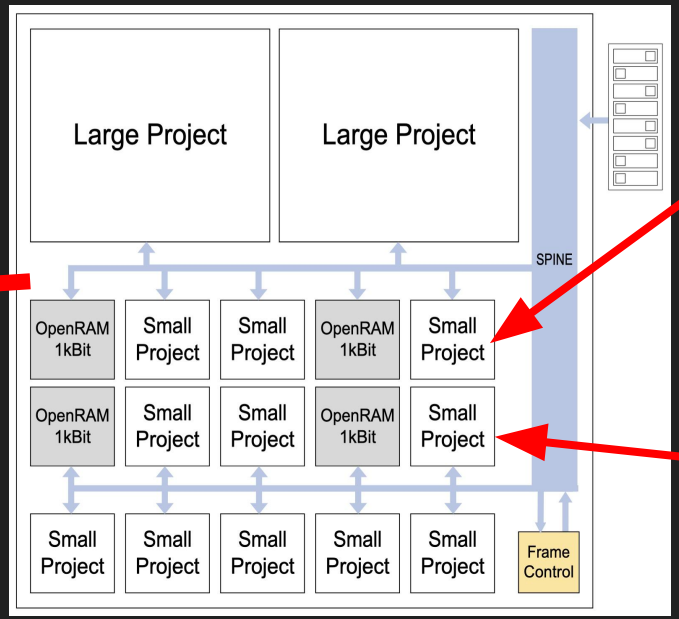

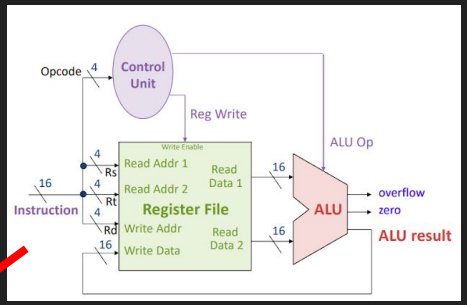

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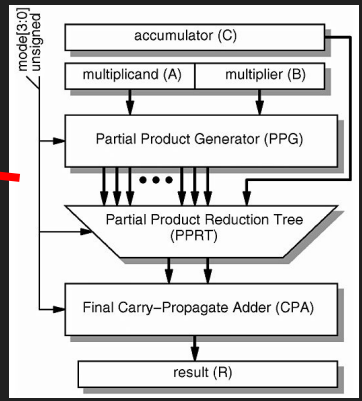

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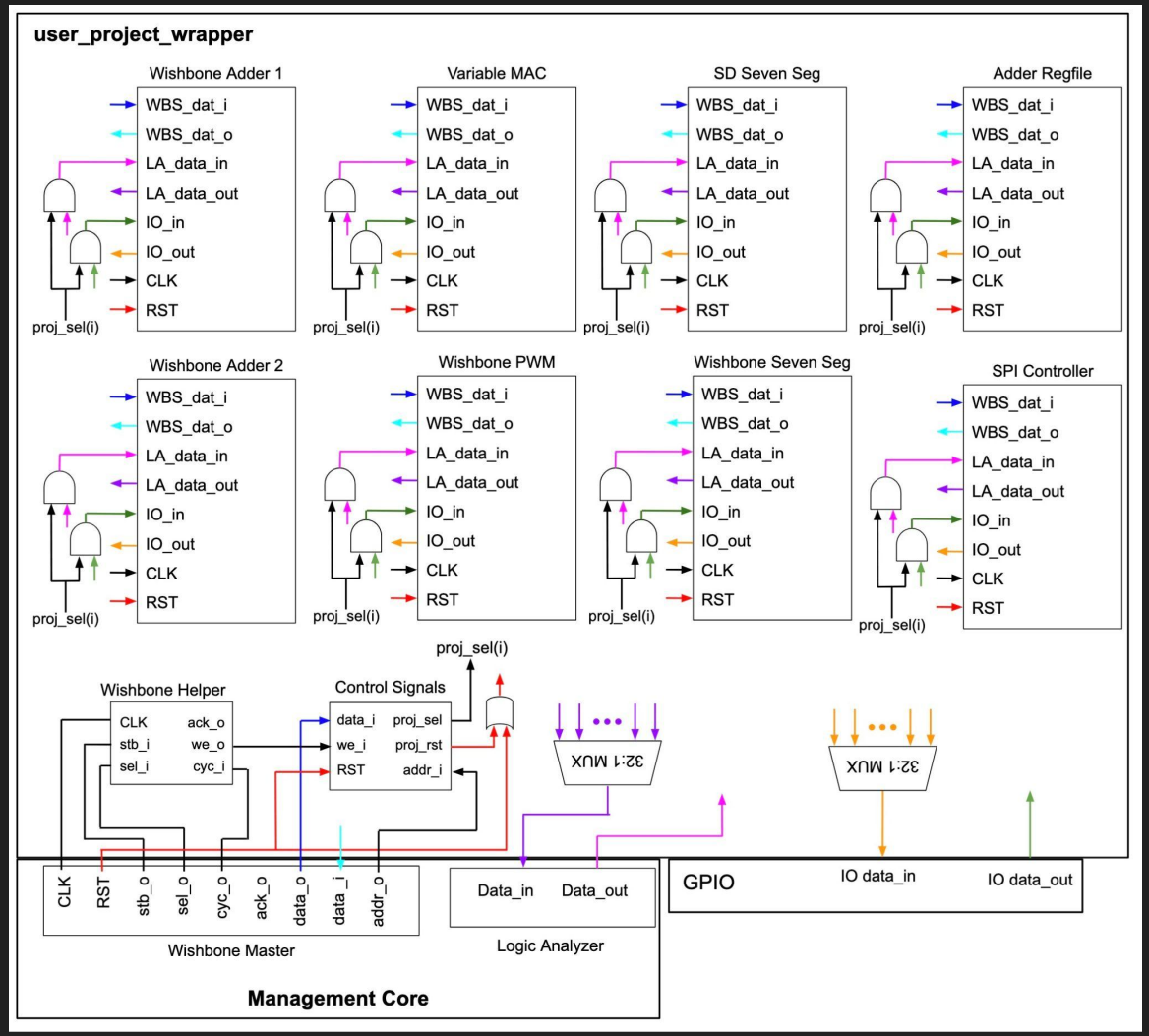
Design Schematic



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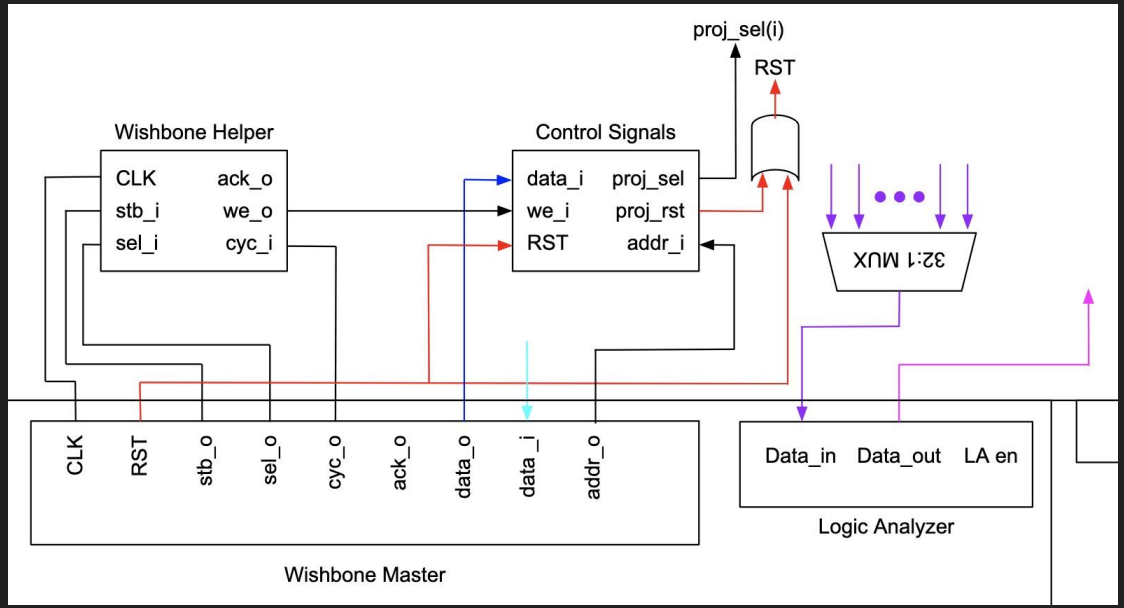
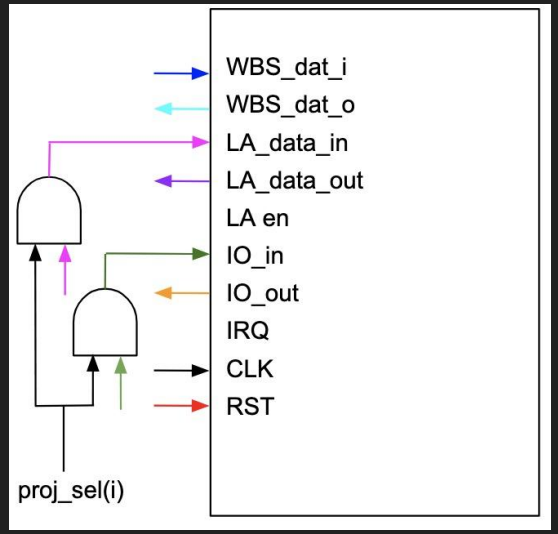
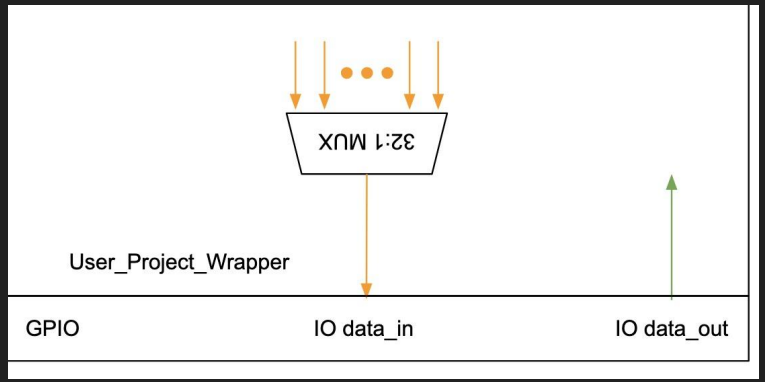
Configuration Logic







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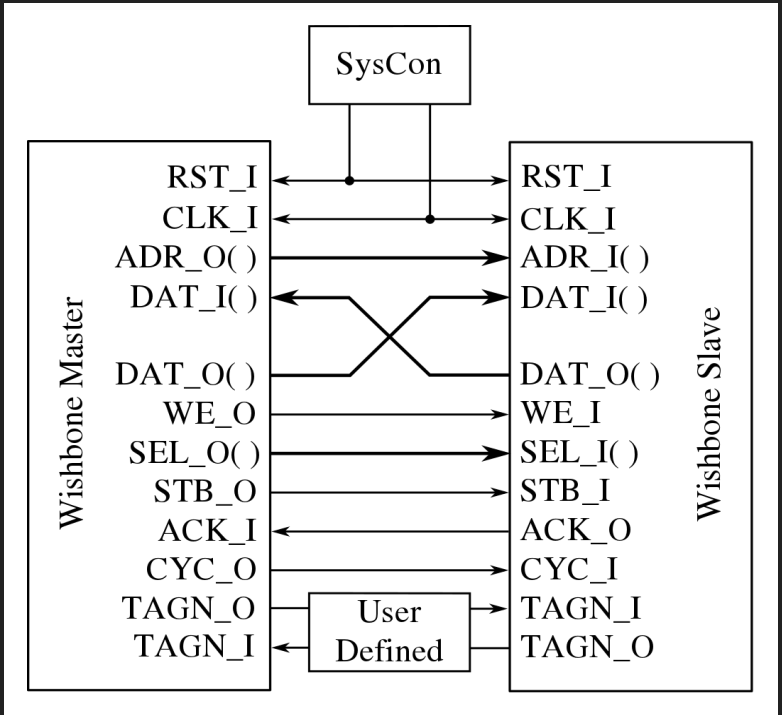
Interfaces

- **Wishbone Bus**
  - Interface between microcontroller and user projects
- **Logic Analyzer Probes**
  - Signals driven or monitored by microcontroller
- **Input/Output Ports**
  - Programmable pins to send or receive data externally



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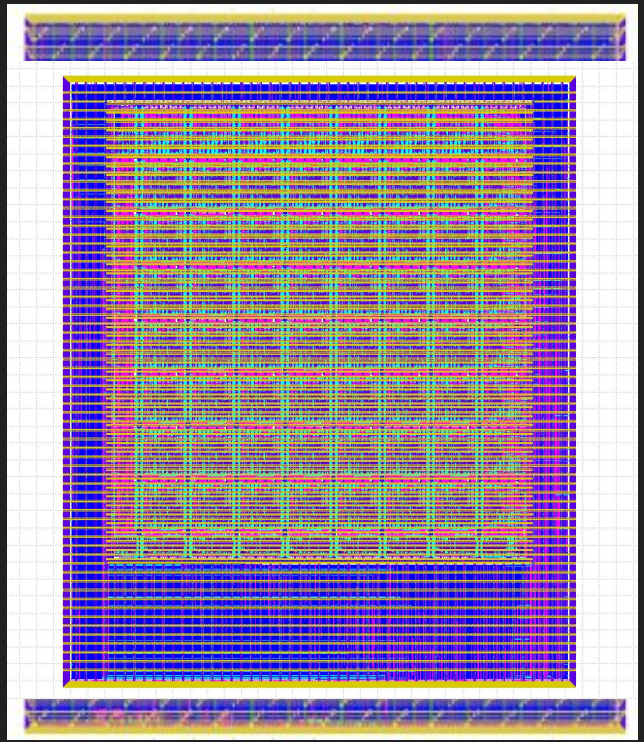
Top-Level Integration

- **Method 1** – Macro-First Hardening
  - All macros are hardened and placed in wrapper
- **Method 2** – Full-Wrapper Flattening
  - All user logic placed directly in wrapper
- **Method 3** – Top-Level Integration
  - Hardened macros and additional logic placed in wrapper



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Hardening Method

- Method 3 - Top-Level Integration
  - Minimum student project die area = 501 x 501 µm
  - $10mm^2$ / $.25mm^2$ = ~40 possible projects
- Method 2 - Full-Wrapper Flattening
  - No minimum project die area

Component	Run #	Changed Settings	# Ports	CLOCK_PERIOD	CLOCK_PORT	CLOCK_NET	FP_SIZING	DIE_AREA	PL_TARGET_DENSITY	Pass? (Y/N)
adder_wrap	1	-	607	25 (40 MHz)	wb_clk_i	[blank]	absolute	0 0 700 700	0.55	Y
adder_wrap	2	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 350 350	0.55	N
adder_wrap	3	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 525 525	0.55	Y
adder_wrap	4	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 438 438	0.55	N
adder_wrap	5	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 482 482	0.55	N
adder_wrap	6	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 500 500	0.55	N
adder_wrap	7	DIE_AREA	607	25	wb_clk_i	[blank]	absolute	0 0 501 501	0.55	Y

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Risk Mitigation

Risk	Mitigation
External SRAM Integration	Remove OpenRAM and add DFF RAM if time permitting.
Cannot complete design before tapeout deadline	Schedule meetings with Efabless group to get assistance with errors/issues in the design.
Projects and spine do not fit into user space	Decrease the required number of projects to be implemented into our design.
Post fabrication errors	Complete testing of our design before tapeout submission including Verilog and C++ test code.

Testing Plan

- **Unit Testing** - Simulations for individual projects
- **Integration Testing** - Simulations for entire framework
  - Project selection, switching, reset
  - Maintaining individual project functionality
- **Acceptance Testing** - Hardening and Precheck
  - Optimal hardening configuration
  - Timing issues/concerns
- **Bringup Testing** - Future testing plan

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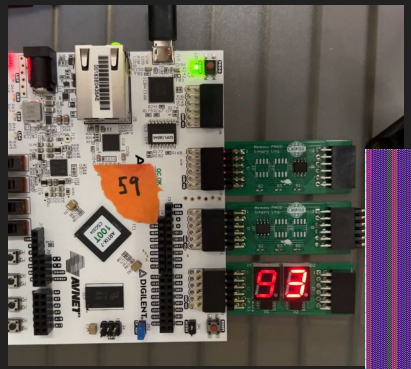
Testing Steps

- **Simulations & Emulations**
  - RTL, GL
  - C code, FPGA
- **Hardening**
  - Place and route
  - Static Timing Analysis (STA)
- **Precheck**
  - Required for Efabless submission
  - Layout Versus Schematic (LVS)
  - Design Rule Check (DRC)
- **Bringup**
  - Re-use C code



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Testing Results

Step	Status
Project Simulations	Pass (RTL, GL, FPGA)
Project Hardening	Pass
Framework Simulations	Pass (RTL, GL, FPGA)
Framework Hardening	Pass with Timing Warnings
Framework Precheck	Pass
Tapeout	Pass

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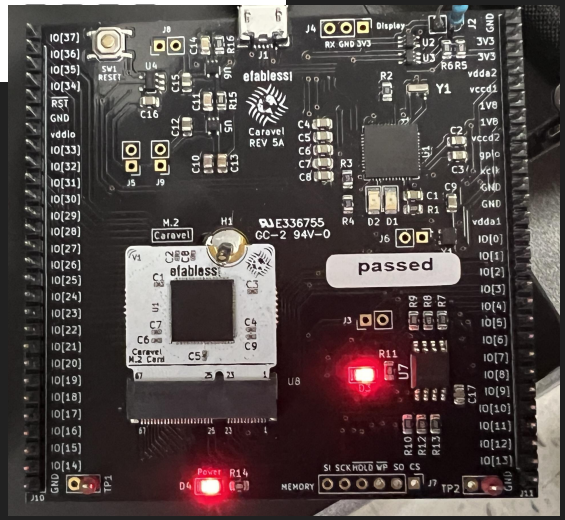
Static Timing Analysis Results

- Max hold, slew, capacitance violations
  - Non-critical timing paths - LA pins to/from IO pins
- Chip-level STA runs
  - Clock frequency - 40 MHz, 10 MHz
  - Max slew and capacitance margins
- Opportunity for debug analysis
  - Explore timing issues
  - Variation between chips

Future Impact

- Chip is currently being fabricated
- ISU ASIC Expansion
  - Bringup experience
  - More resources for Chip Forge
- New Programs
  - Potential undergraduate course incorporation
- Industry connections
  - Internship and full-time opportunities



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References

[1] https://fr.wikipedia.org/wiki/GTKWave

[2] https://github.com/klayout

[3] https://efabless.com/open_shuttle_program

[4] https://caravel-harness.readthedocs.io/en/latest/

[5] https://cs.wellesley.edu/~cs240/s24/lab/lab05/notebook.html

[6] https://www.researchgate.net/figure/Block-Diagram-of-a-MAC-Unit_fig4_342692405

[7] https://en.wikipedia.org/wiki/Wishbone_(computer_bus)

[8] https://info.efabless.com/knowledge-base/top-level-integration-and-power-management

Thank you!

Questions?