# Digi Nitoboll

# **Digital ASIC Fabrication**

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Group: sddec24-12

## Client & Faculty Advisor: Dr. Henry Duwe

Introduction	Intended Users			
<ul> <li>Undergraduate students rarely have the opportunity to design, fabricate, and bring-up custom application-specific integrated circuits (ASICs)</li> <li>Chip Forge - Co-curricular team at ISU for students, freshmen through</li> </ul>	<b>l.</b> Future Students	Profes	2. ssors & cators	<b>3.</b> Open-Source Community
seniors, interested in chip fabrication Purpose	Requirements			
<ul> <li>Create framework to fabricate multiple student projects on the same chip</li> <li>Support Chip Forge and continuous cycle of tapeouts</li> <li>Amortize cost of fabrication</li> </ul>	<ul> <li>Supports up to 15 total projects</li> <li>Software on microcontroller selects which project is active</li> <li>One project is active at a time</li> <li>Projects interface with Wishbone bus, LA pins, and IO pins</li> </ul>			
Development Process	<ul> <li>Design successfully president of the second s</li></ul>	passes preche	eck and tapeor	ut
Design Specification RTL Design Verification Synthesis	Technical Details			
	Wishbone Adder 1	Variable MAC	SD Seven → WBS_dat_i	Seg Adder Regfile
Bringup Tapeout + Sign-off + Hardening	WBS_dat_o LA_data_in LA_data_out	WBS_dat_o LA_data_in LA_data_out	WBS_dat_o	WBS_dat_o LA_data_in LA_data_out



## **Design Approach**



- Spine controls data flow and communication between projects and microcontroller
- Projects have full access to chip interfaces through multiplexing
- Fully isolated projects with independent selection and reset
- Integrate actual projects created by students in Chip Forge
- Initial plans for external SRAM with OpenRAM macros

## Results

#### Implementation

• Design fully implemented in Verilog, with student projects integrated

#### Testing

- User projects passed unit tests and integration tests inside framework
- Design passed precheck and tapeout locally and on Efabless server

#### Tapeout

• Design submitted for fabrication on

IO\_out IO\_out IO out IO\_out CLK CLK CLK CLK RST RST RST RST proj\_sel(i proj\_sel(i roj sel( Wishbone PWM Wishbone Seven Seg Wishbone Adder 2 SPI Controller → WBS\_dat\_i → WBS\_dat\_i → WBS\_dat\_ → WBS\_dat\_i WBS\_dat\_o WBS\_dat\_o WBS\_dat\_o WBS dat o LA\_data\_in LA\_data\_in LA\_data\_in LA\_data\_in LA data out LA data out LA data out LA\_data\_out IO in IO in IO in IO in IO\_out IO out IO\_out IO out CLK → CLK CLK - CLK RST RST RST RST proj\_sel(i proj\_sel(i proj\_sel(i proj\_sel(i) proj\_sel(i **Control Signals** Wishbone Helper proj\_sel ... data i CLK ack\_c ... stb we\_c proj\_rst 32:1 MUX 32:1 MUX cyc\_i sel\_i RST addr i IO data\_in GPIO IO data\_out CLK data\_i tb o сқ\_о Ita\_0 RST yc\_o Data in Data out

IO in

IO in

#### Interfaces

• Wishbone bus, Logic Analyzer (LA) pins, Input/Output (IO) Pins

IO in

#### **Open-Source Development**

Wishbone Master

IO in

Efabless Caravel architecture, SkyWater 130nm Open-Source PDK

Logic Analyzer

## Testing

#### **Simulations and Emulations**

Register Transfer Level (RTL) simulations

**Management Core** 

- Gate-Level (GL) simulations with synthesized netlist
- Verilog testbenches and C code to program microcontroller

November 11th deadline

• Fabricated chip will be brought up by Chip Forge in the spring

#### 8 Included Projects:

- Wishbone Adder x2
- Variable MAC
- Sr. Design Seven Seg. Display
- Wishbone Seven Seg. Display
- Adder Register File Datapath
- PWM Controller
- SPI Controller



Hardened Design Submitted for Tapeout

### **Future Impact**



#### **ISU ASIC Expansion**

- Bringup experience with physical chip
- Foundation for future tapeouts

#### **New Programs**

• Potential undergraduate course incorporation

#### **Industry Connections**

• Internship and full-time opportunities

• FPGA emulations for further pre-fabrication testing

#### Hardening and Precheck

- Required for Efabless tapeout submission
- Ensures design will function as expected post-fabrication
- Place and route, Static Timing Analysis (STA), Layout Versus Schematic (LVS), Design Rule Check (DRC)

#### Bringup

- Re-use C code for bringup board tests to verify physical chip
- Framework user guide and example hardening configurations



#### FPGA Test of Seven Segment Display Project

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