Digital ASIC Fabrication

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Introduction

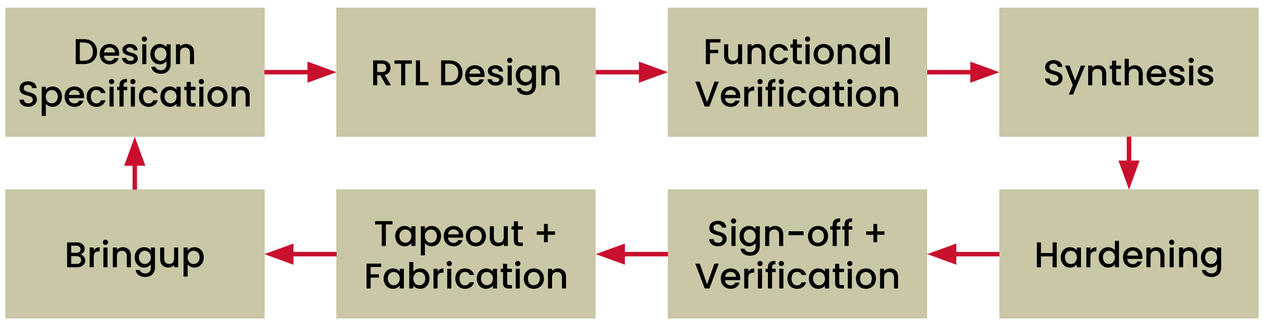
Context

- Undergraduate students rarely have the opportunity to design, fabricate, and bring-up custom application-specific integrated circuits (ASICs)
- Chip Forge - Co-curricular team at ISU for students, freshmen through seniors, interested in chip fabrication

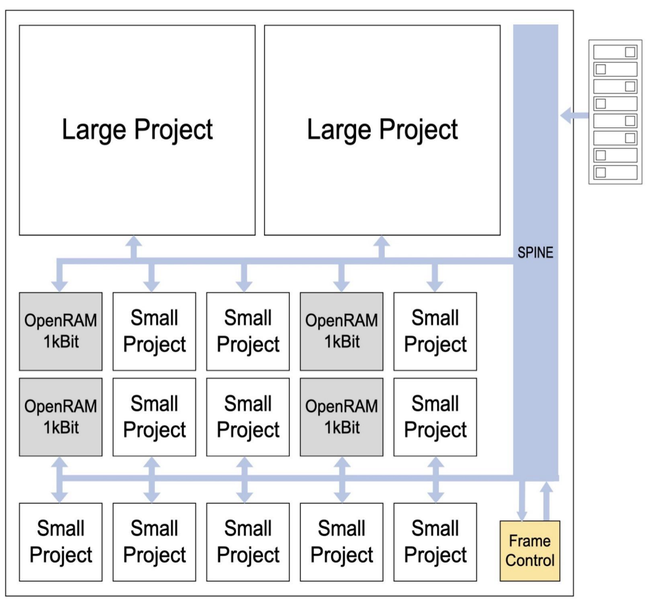
Purpose

- Create framework to fabricate multiple student projects on the same chip
- Support Chip Forge and continuous cycle of tapeouts
- Amortize cost of fabrication

Development Process



Design Approach



- Spine controls data flow and communication between projects and microcontroller
- Projects have full access to chip interfaces through multiplexing
- Fully isolated projects with independent selection and reset
- Integrate actual projects created by students in Chip Forge
- Initial plans for external SRAM with OpenRAM macros

Results

Implementation

- Design fully implemented in Verilog, with student projects integrated

Testing

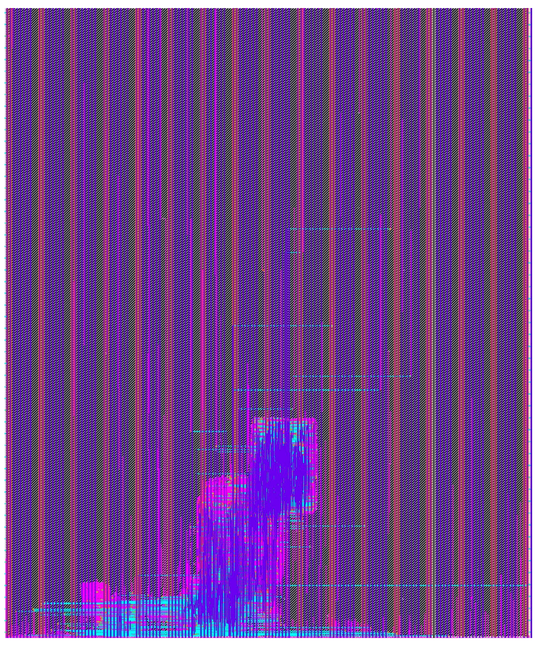
- User projects passed unit tests and integration tests inside framework
- Design passed precheck and tapeout locally and on Efabless server

Tapeout

- Design submitted for fabrication on November 11th deadline
- Fabricated chip will be brought up by Chip Forge in the spring

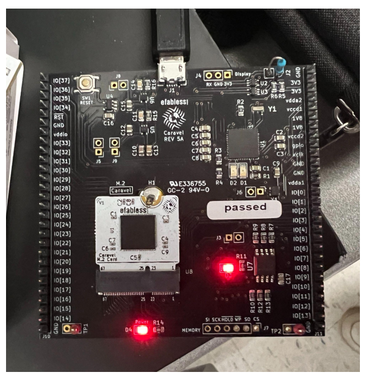
8 Included Projects:

- Wishbone Adder x2
- Variable MAC
- Sr. Design Seven Seg. Display
- Wishbone Seven Seg. Display
- Adder Register File Datapath
- PWM Controller
- SPI Controller



Hardened Design
Submitted for Tapeout

Future Impact



ISU ASIC Expansion

- Bringup experience with physical chip
- Foundation for future tapeouts

New Programs

- Potential undergraduate course incorporation

Industry Connections

- Internship and full-time opportunities

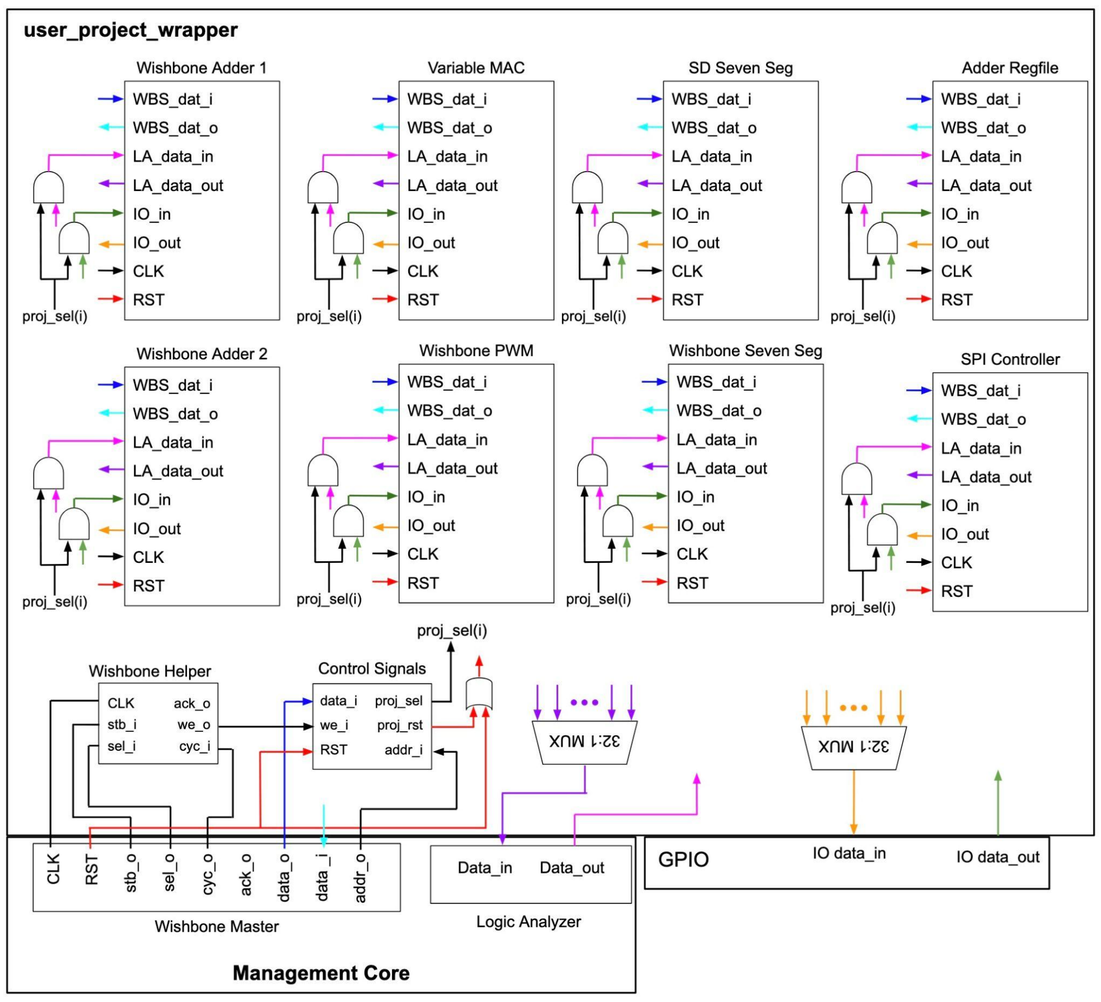
Intended Users

1. **Future Students**
2. **Professors & Educators**
3. **Open-Source Community**

Requirements

- Supports up to 15 total projects
- Software on microcontroller selects which project is active
- One project is active at a time
- Projects interface with Wishbone bus, LA pins, and IO pins
- Design successfully passes precheck and tapeout

Technical Details



Interfaces

- Wishbone bus, Logic Analyzer (LA) pins, Input/Output (IO) Pins

Open-Source Development

- Efabless Caravel architecture, SkyWater 130nm Open-Source PDK

Testing

Simulations and Emulations

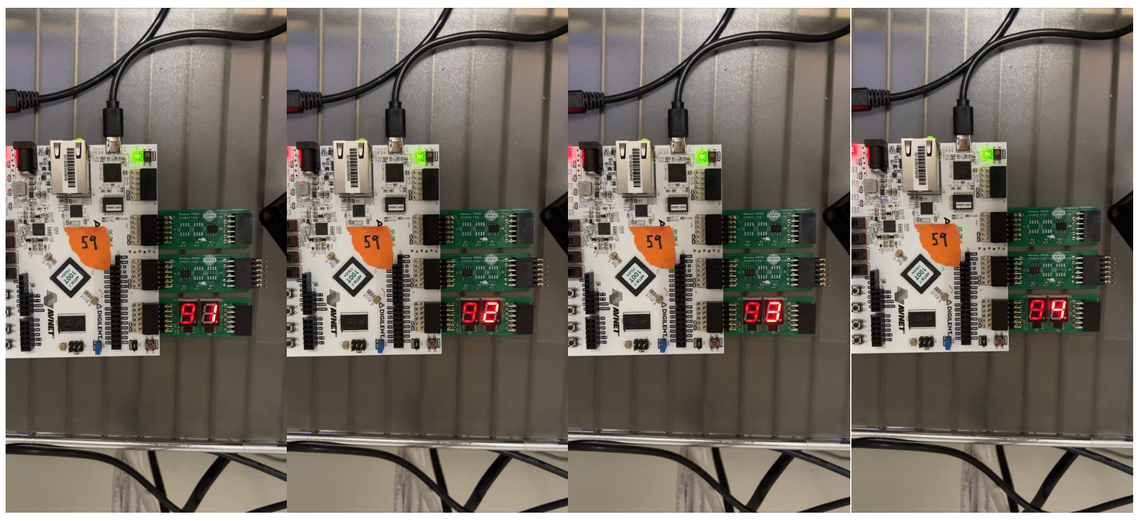
- Register Transfer Level (RTL) simulations
- Gate-Level (GL) simulations with synthesized netlist
- Verilog testbenches and C code to program microcontroller
- FPGA emulations for further pre-fabrication testing

Hardening and Precheck

- Required for Efabless tapeout submission
- Ensures design will function as expected post-fabrication
- Place and route, Static Timing Analysis (STA), Layout Versus Schematic (LVS), Design Rule Check (DRC)

Bringup

- Re-use C code for bringup board tests to verify physical chip
- Framework user guide and example hardening configurations



FPGA Test of Seven Segment Display Project