EE/CprE/SE 491 WEEKLY REPORT 9

Digital ASIC Fabrication

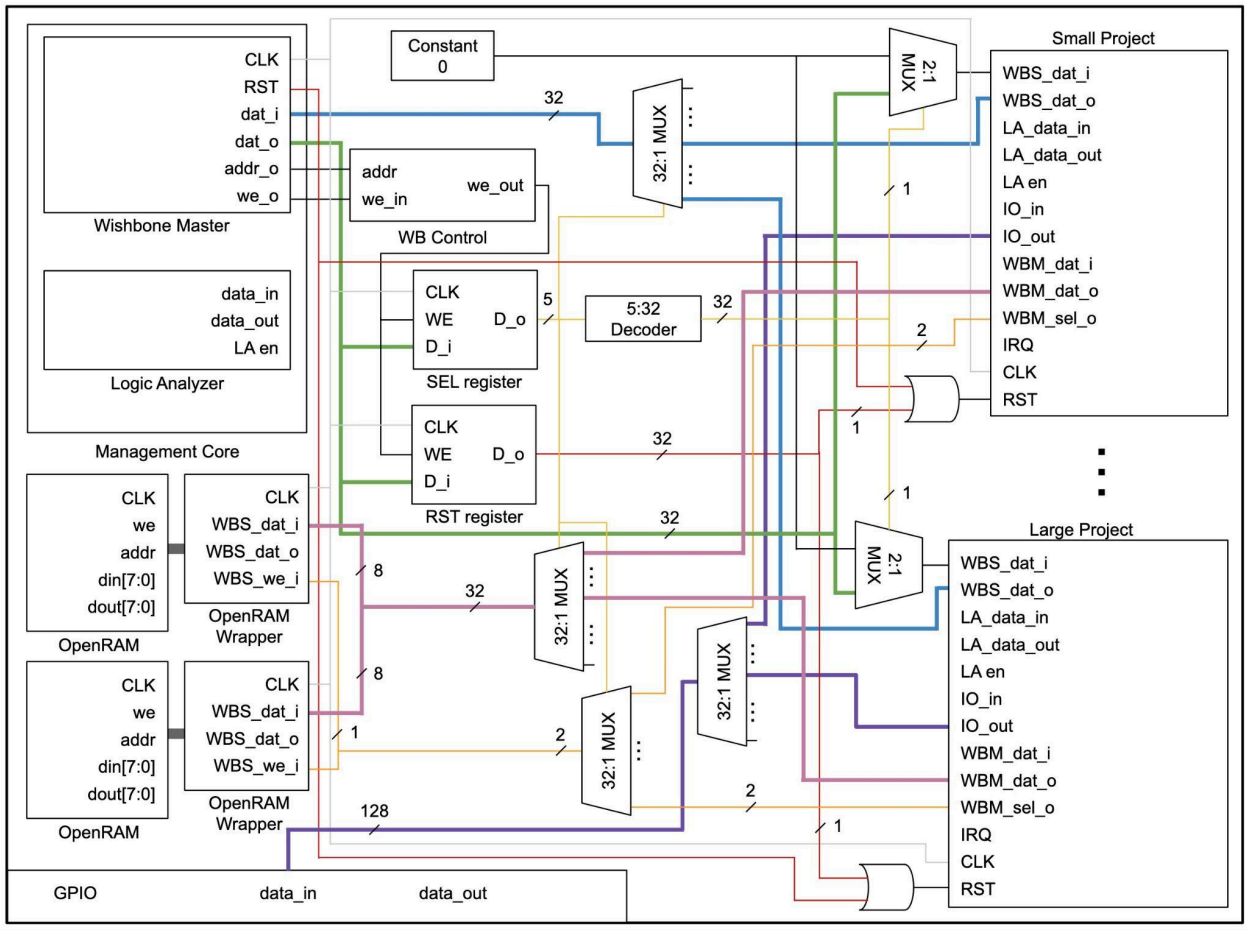
April 2, 2024 – April 9, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary



Past Week Accomplishments

- **Mitchell:** I began debugging the decoder. I had to rewrite the code as I switched from (if else) statements to (case statements). I am still debugging this code.
- **Evan:** I wrote a bash script that either: adds functional include statements in $PWD/verilog/includes/*, adds an empty verilog file in $PWD/verilog/rtl and a testbench in $PWD/verilog/dv OR deletes the includes, and (optionally) deletes the files and folder from the directory hierarchy. This can be expanded, but currently, it works as advertised.
- **Baoshan:** I built a testbench code of decoder 5 to 32 and simulated it. I also tried using several decoders combined into a 5 to 32 decoder. The waveform works as expected.
- **Katie:** I created an updated design schematic that includes OpenRAM modules. Ran into a few questions about the interconnection between OpenRAM, projects, and the Wishbone protocol (see below). I also ran more hardening configurations with the additional Wishbone master ports on the projects and found the minimum required die area. I tried experimenting with different clock frequencies, but they consistently resulted in max fanout violations, including the default clock period (25 ns).

Pending Issues

- **Mitchell:** I had trouble getting past syntax errors dealing with if, else if statements. I looked through many examples, and there wasn't a straightforward answer. Creating a Verilog standards document may be helpful not just for our team with these issues but for other teams in the future.
- **Evan:** I need to get caught up from last week and familiarize myself with OpenRAM and its implementation. Maybe implement OpenRAM in something to demonstrate functionality. Depends on availability.
- **Baoshan:** Combine a 2 to 4 and a 3 to 8 decoder. There are some problems with the use of wire. The same variable name is used in different modules.
- **Katie:** Will we be modifying the existing OpenRAM modules to have just 1 R/W port? Will the wishbone slave ports on the OpenRAM wrapper have 32 or 8 bit data ports? When will the four, 8-bit data outputs get concatenated into the 32 bit signal? For the WB interface, will we be including all the WB ports?

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	I began debugging my code and thinking about some Verilog standards that could be useful for our team.	8	40
Evan	Script + catching up.	5	36
Baoshan	Testbench and practice	3	33
Katie	Updated design schematic with OpenRAM, hardening data	6	43

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Make more modules, implement a simple openRAM module in a top-level wrapper, and experiment with the wrapper and BUS. Maybe harden things.	Evan	5/x/24
Harden user_project_wrapper	Katie	4/x/24
Harden the decoder and prove simulates with register file data as input.	Mitchell	4/16/24
	Baoshan	4/x/24

Advisor Meeting Summary

Create a top-level ‘framework’ or interface for testing purposes, from which we can then design the implementation with OpenRAM and how we’ll plug in modules.