EE/CprE/SE 491 WEEKLY REPORT 8

Digital ASIC Fabrication

March 26, 2024 – April 2, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

This week, we continued to experiment with hardening configurations and develop and test new modules. We also began researching how to incorporate OpenRAM modules into our overall design.

Past Week Accomplishments

- **Mitchell:** Created a 5:32 bit Decoder to select which project will be active in our framework. Working to simulate and harden.
- **Evan:** I worked on shrinking the logic analyzer project inside the wrapper, in addition to playing around with the configuration file. CSVs are in the metrics folder.
- **Baoshan:** I am writing Verilog code for a 5:32 decoder and trying to harder it. Additionally, I am investigating the OpenRAM module to learn more about it
- **Katie:** I experimented with different hardening configurations for a project wrapper with all required ports, specifically the die area. I documented all my results in the Hardening Data sheet. I attempted to harden the user_project_wrapper, but ran into more issues. Currently trying to debug those with Jake's help. I also started looking into OpenRAM to understand how to integrate it into our framework design. I had some questions about how we want to use OpenRAM in our framework.

Pending Issues

- **Mitchell:** Had issues with the makefile and simulating the decoder. I was working around these issues but had limited time with exams.
- **Evan:** Many of the modules we'll need are unimplemented as of yet.
- **Baoshan:** I have completed editing the code but have not yet created the testbench. Also I don't quite know the purpose of some modules. I may need to look into this some more.
- **Katie:** How many OpenRAM modules are we looking to include in our framework? Is there a minimum/set number of RW and R ports we want to include on each module? Number of additional ports needed on each user project will be dependent on this.

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Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Created a 5:32 bit decoder in Verilog. Working on simulating and hardening.	4	32
Evan	Die area, configuration file parameters, and shrinking projects while maintaining functionality. Various hardening techniques	5	31
Baoshan	Code for decoder. Study the content of openram. research schematic	4	30
Katie	Experimented with hardening configurations, documented results, learned about OpenRAM	5	37

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Make more of the Verilog modules we'll need, and find a minimum functional level for their own respective functionality.	Evan	5/x/24
Harden user_project_wrapper, integrate OpenRAM into design composition	Katie	4/9/24
Harden the decoder and add it to Git for the team to see. Work on using the decoder with a 32:1 MUX to select which data is being input into the Wishbone.	Mitchell	4/9/24
Complete the Verilog module and contact the content of openRam	Baoshan	4/9/24

Advisor Meeting Summary

- Want to have different user clock frequencies for different projects
    - User clock is separate from the wishbone clock
- Incorporate the existing OpenRAM modules into our design for now
    - Use four 8-bit modules to store 32 bits of data
- Use Wishbone protocol to connect OpenRAM modules and user projects
    - User projects will be masters, OpenRAM modules will be slaves
    - Want the ability to enable 1 OpenRAM module at a time