EE/CprE/SE 491 WEEKLY REPORT 7

Digital ASIC Fabrication

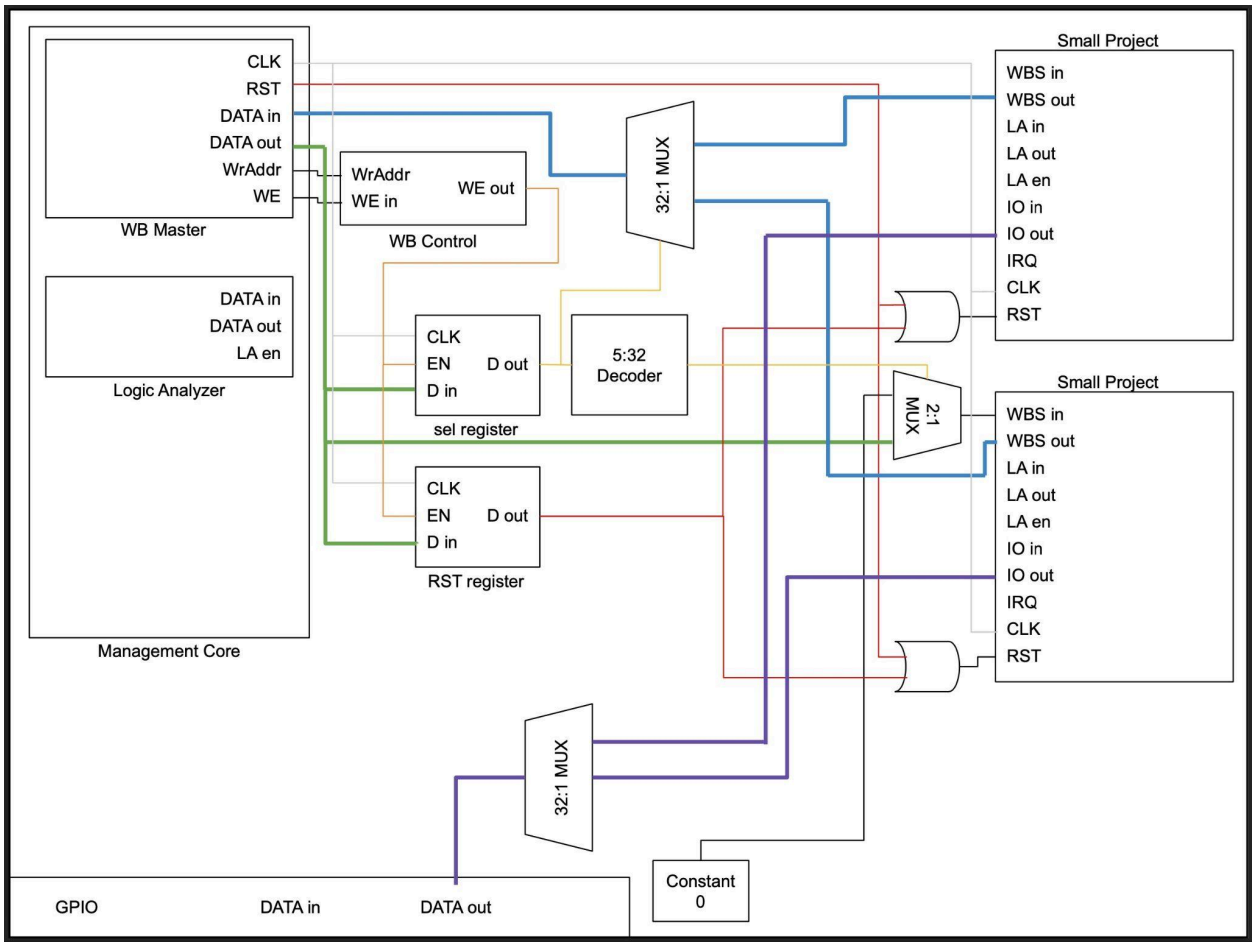
March 20, 2024 – March 26, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary



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Past Week Accomplishments

- **Mitchell:** Continued working with adder and MUX to get hardened.
- **Evan:** This week there was significant progress made. I finished debugging my module from last week, have delved deeper into the Caravel tutorials, thereby messing around with the die area of my inverter and register projects just as an experiment. I ran into issues during the hardening process when I started. Moreover, I'm reading (and may be done with by the time we meet) the documentation regarding writing arbitrary values from the GPIO pins into my project via the wishbone bus.
- **Baoshan:** Since I missed the last meeting, I continued working on what I had started last week, which involved designing the decoder and multiplexer modules using schematic diagrams. Additionally, I researched more information about inputs and outputs and connection between various modules.
- **Katie:** I implemented the changes we talked about last meeting in the design schematic. I also tried hardening a user_project_wrapper with multiple modules instantiated, but ran into some errors.

Pending Issues

- **Mitchell:** N/A
- **Evan:** Learning more about the WB-BUS, wiring it up, the hardening process, and various size limitations for modules. Maybe look into adding memory? Also - I will not be here next week (4/2).
- **Baoshan:** Understand the functions of each module and how they are connected.
- **Katie:** What is the proper way to hardcode module outputs to 0? How do you resolve a hardening error about netlist mismatch? After looking at the log files, it seems like the only mismatching ports were vccd1 and vssd1.

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Continued working with adder and MUX to get hardened.	2	28
Evan	Experimented with Die area. RTL simulations. Looking into getting a minimal version of the BUS implemented and wired with a few trivial projects. Finished and tested successfully an N-bit register.	6+	26
Baoshan	Build multiplexers and decoders. Find more useful information. Effectively connect various modules.	4	26
Katie	Design decomposition, project wrapper hardening	5	32

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Complete my IO project. Get a bare bones WB-BUS implemented myself(?) and get it wired up. Further jump into the die area and how this impacts the hardening process. Fix bugs related to the hardening process.	Evan	3/X/24-4/X/24
Hardening project wrapper, try different configurations	Katie	4/2/24
Finish and clean up 2to1MUX and Adder. Look into the decoder and 32to1MUX.	Mitchell	4/2/24
Know the input and output directions of each module.	Baoshan	4/2/24

Advisor Meeting Summary

- Create a modular ‘wrapper’ - Effectively create a known quantity which we then provide instructions for adapting user’s projects towards
    - This will be what is connected to the wishbone bus.
- OpenRAM ‘prehardened’ modules are provided a ‘dependency’ folder. - These should be looked into.
    - Prioritize creating tables of hardening data, the size of various modules and their alignment for our presentation come the end of March/dead week.
    - These are the most important aspects which should supersede all others.