Digital ASIC Fabrication

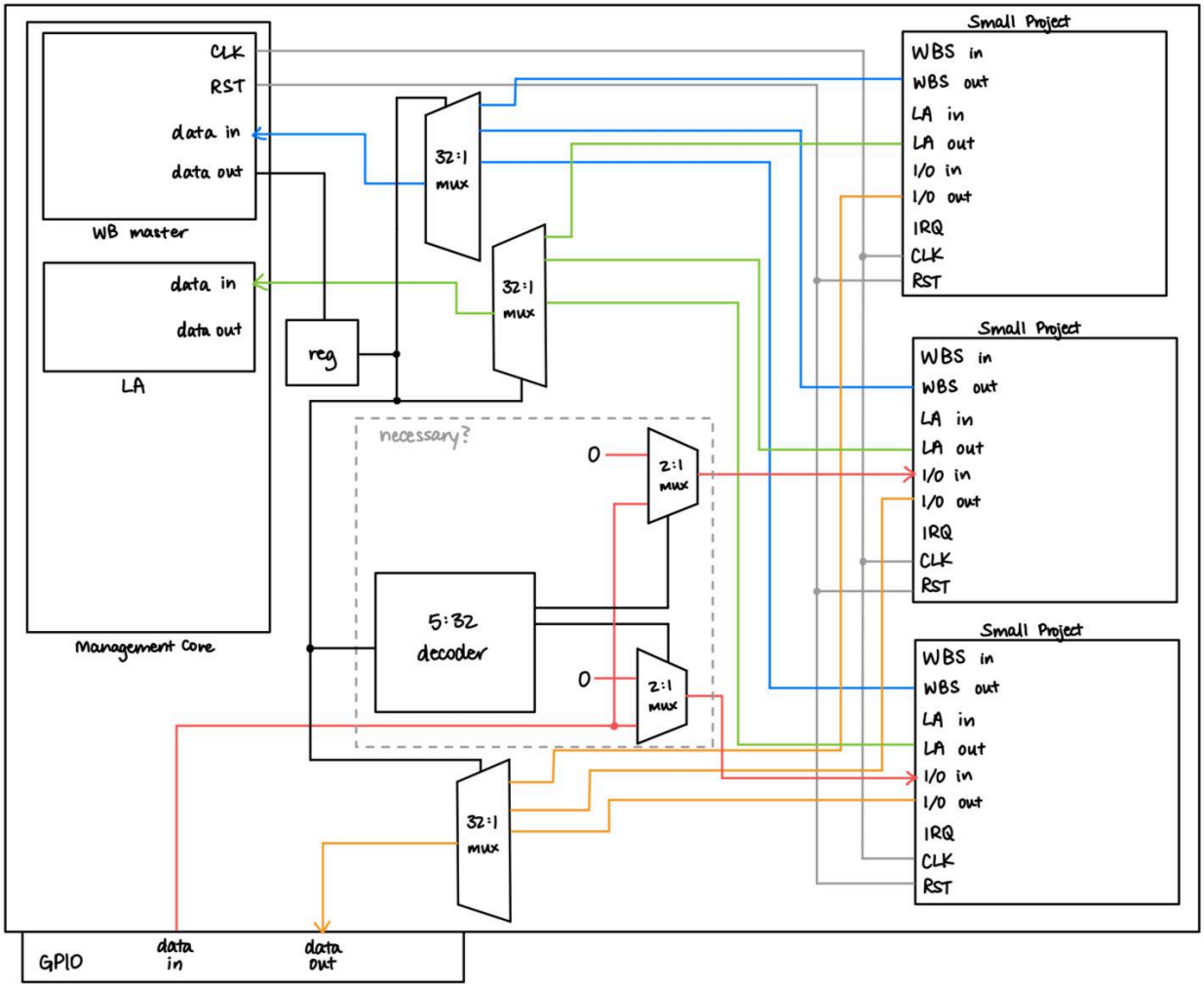
March 5, 2024 – March 19, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary



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Past Week Accomplishments

- **Mitchell:** Created C files for 2to1MUX and adder. Created test benches for the mux and adder and implemented them within the caravel wrapper. I was able to run and view waveforms for the adder.
- **Evan:** This week I created modules for a single bit register, and a module to instantiate that N times - thereby creating an arbitrary width storage medium within the program. I also created a testbench. As of right now, I believe the single bit register is working, however there is still some finetuning that needs to be done to fix the n bit instantiation.
- **Baoshan:** This week, I studied the schematics, reviewed and executed the .v files, and experimented with the 2-to-1 multiplexer and decoder. Comparing the waveform diagram after simulation, it aligns with my initial concept.
- **Katie:** I began creating a first draft of our design composition, shown above. The schematic is general and doesn't include every project or wire. I made some assumptions based on questions I had, specifically about connecting signals to project inputs (see Pending Issues).
    - I assumed projects did not have enable signals, and that their inputs needed to be 0 if not currently enabled.
    - My initial idea for the input connections is shown in the dashed box and utilizes a decoder and multiple 2:1 muxes.
    - If the data inputs on inactive projects don't matter, then the data inputs can connect directly to the projects, and the decoder/2:1 muxes can be removed.
    - Since I wasn't sure about my assumptions, the data input signals from the logic analyzer and wishbone bus are not drawn out at the moment but would be the same as the GPIO connection.

  I also added a single register to hold the signal controlling which project is active. I plan to add a Wishbone control module that will handle reading in that value from the Wishbone bus.

Pending Issues

- **Mitchell:** I am unsure if all my signals/waves are correct. I need to take a deeper look into my outputs and run the simulation for my MUX. I was shown an example that has sped up how fast I can create and run simulations.
- **Evan:** As mentioned previously, the n bit addition to my register doesn't work - or that being, the generate function doesn't properly connect it. Currently my register works, and thus presumably the n bit version works as well, I just need to find out why the reg vector doesn't properly connect (and thus display on the waveform).
- **Baoshan:** Although the mux module was created, it was not clear what should be connected to the output, how to control the input signal, and the conversion of digital and analog signals.
- **Katie:** Will each smaller project have an enable signal? Will inputs to smaller projects need to be 0/high impedance for inactive projects?

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Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Created 2-to-1 MUX and adder in C, which can be simulated with the caravel wrapper.	7	26
Evan	N bit register, 1 bit register. Looking into pins via the C code (very limited, will revisit).	6	20
Baoshan	Write the code of the module and generate the v file. The waveform was successfully simulated.	4	22
Katie	Design schematic	5	27

Plans for the Upcoming Week

Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.

Action Item	Person in Charge	Expected Date
	Evan	3/26
Continue working on design decomposition, make changes talked about in the meeting, add wishbone control module	Katie	3/26/24
Finish and clean up 2to1MUX and Adder. Look into the decoder and 32to1MUX.	Mitchell	3/26/24
Know the input and output directions of each module.	Baoshan	

Advisor Meeting Summary

- Inputs to inactive projects should be 0
- Don’t reset inactive projects. Want them to hold their state unless explicitly reset
- Have a separate reset pulse, independent from the wishbone reset
    - This will reset just the active project
- Revisit clock gating and power gating in the future.
    - “Disabling” the clock on inactive projects will save energy.