EE/CprE/SE 491 WEEKLY REPORT 5

Digital ASIC Fabrication

February 28, 2024 – March 5, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

We have started to research the different components that will be used in our final design and plan our overall design. We are also working on creating new example designs that interface with GPIO ports and signals to test simulating and hardening ourselves.

Past Week Accomplishments

- **Mitchell:** Began implementing MUX, Adder, and Register in Verilog. Researched/googled Verilog formatting/style.
- **Evan:** Very little other than planning for an aforementioned project involving simple half word inputs/outputs to an LED board from a module. Hereafter referred to as the LED module.
- **Baoshan:** I practice a project from a sample to seven segment seconds. Wrote Verilog code. Hardening I don't quite understand, but I need to practice more. Changing something to see what happens.
- **Katie:** I started researching the different design components that will be used in our design, including the harness, management SoC and wishbone bus. I also looked through the design documents and source files from previous semesters to better understand how the components are connected.

Pending Issues

- **Mitchell:** Testing of Verilog code and implementing it into the caravel repo.
- **Evan:** Physical designing of the LED module and the majority of the work. I plan to put significant, tangible work into it during spring break. Moreover this is unrelated explicitly to the project technically, but I have a significant lack of free time.
- **Baoshan:** Get waveform after successfully verifying Verilog code. Get .v file
- **Katie:** There are some aspects about the different components and how they work together that I am a little unclear about. I will ask for clarification during our weekly meeting.

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Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	I began writing code in Verilog for 2to1 MUX and Adder. Read some formatting for Verilog code.	3	19
Evan	Design only, as well as completed biography on the team website. Little tangible progress except for outlining components and some very tentative sketching of the Verilog components.	3	14
Baoshan	Practiced seven segment Verilog code and studied the design process of graduates	4	18
Katie	Component and interface research	4	22

Plans for the Upcoming Week

Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.

Action Item	Person in Charge	Expected Date
More work on LED module design, implementation.	Evan	3/X/24
Research interconnection between components, begin creating design composition; look at adder design	Katie	3/19/24
Simulate MUX and Adder	Mitchell	3/19/24
Get waveform	Baoshan	3/19/24

Advisor Meeting Summary

Advisor notes that we should have more concrete deliverables when coming to meetings. Specific examples of research/progress in order to gauge progress over time, as well as to notate decisions taken. This by means of encouraging us to further document our progress, design in order to review the final outcome of our project.

Do the minimum first; add complexity later. Secondarily, do not under any circumstances use the openRAM until there is a tutorial available. Finally, add peripherals only under absolute duress.

BIts can be configured as either input or output.

Small registers to take input from wishbone bus. This is so data is saved between cycles.