EE/CprE/SE 491 WEEKLY REPORT 4

Digital ASIC Fabrication

February 21, 2024 – February 27, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

Short summary of what the group did for the week. This should be about a paragraph in length. These are just a few questions to help you get started. What was the overall objective for the week? In general, what tasks were completed? Were there any changes made to the project?

Past Week Accomplishments

Please describe/summarize what was done, by whom, when, and collectively as a group. This should be about a paragraph or two in length. Bulleted points are acceptable as well. Please keep only your technical details related to your project. Figures, schematics, flow diagrams, pseudocode, and project-related results are acceptable, but please ensure they are legible (clear enough to read) and explain. If researching a topic, please add details about what was learned and its relevance to the project. If two or more people worked on a single task, distinguish how each member contributed. Specific details relating to the assistance provided to other members may be included here. Do not include classwork, such as individual reflection assignments and group meetings, as part of your duties.

- **Mitchell:** I went through the example RTL simulation and the example hardening. I attempted the example GL simulation but got errors when attempting the make command. I updated my picture and bio on the team website.
- **Evan:** Simulated and hardened a (simple) custom module I wrote in verilog. It did not connect to any external pins, and only utilized one external module so it was by no means anything complex, but I consider it a start. My next task is to interface with GPIO pins.
- **Baoshan:** I have already conducted RTL simulation and completed the testbench, but I lacked knowledge about hardening. Therefore, I searched for a lot of information to gain a better understanding of it.
- **Katie:** I created our Lightning Talk presentation and added content for all the slides. I also successfully hardened my nor_test module, ran gate-level simulation, and verified its outputs matched the RTL simulation. I ran into a few issues that I was able to debug with Jake's help.

Pending Issues

If applicable: Were there any unexpected complications? Please elaborate.

- **Mitchell:** The GL simulation error delayed how much I wanted to get through this week. Additionally, Downloading the GTKwave app took much longer than I had hoped. I was unable to find just an installer initially but was able to and got the app downloaded.
- **Evan:** Designing a module that integrates both the digital memory module as described in the documentation, but also power, GPIO pins so that I can fully delve into the design process. Additionally, I still do not have GTKwave nor the other requisite software involved in the toolchain, as my time this week has been rather busy.
- **Baoshan:** I don't have much knowledge about the specific steps of hardening, so I've been reviewing a lot of sample code to practice it.
- **Katie:** When trying to run GL simulation on my hardened nor_test module, I encountered issues with the power pins. First, I realized that the GL netlist added VCC and VSS ports to my module, which I then had to add to my original design file. I then had issues correctly assigning the power pins in my testbench to allow GL simulation to run correctly. After getting help from Jake, I learned that VCC should be 1 and VSS should be 0, even if the RTL simulation passed with other values. No outstanding issues, just things to keep in mind going forward.

Individual Contributions

Creating this section is optional, but it is required to include the “Hours Worked for the Week” and their “Total Cumulative Hours” for the project for each member somewhere relevant in your report. Your weekly hours for this course should be 6-8 hours. So please manage your time well. Also, ensure that individual contributions support your claim to the weekly hours. Be honest with the reports.

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	I entered my photo and bio into the team website, Mounted my X-drive, Downloaded and used GTKwave and Klayout, and got through the example GTL simulation and hardening.	5	16
Evan	I (attempted) to insert a custom module into the project. I did not verify that it worked; simply getting it to the harden stage was my priority. NOTE: after consulting with my teammate, I realized that in the future, connecting the power pins et al. is requisite in getting a successful simulation.	4	11
Baoshan	RTL simulation, code for testbench and Practice hardening examples	4	14
Katie	Lightning talk presentation, hardened custom module, ran GL simulation, updated website	5	18

Plans for the Upcoming Week

Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.

Action Item	Person in Charge	Expected Date
Look into the interconnection between components, begin creating design composition	Katie	3/5/24
Interweave modules and at the very least, successfully interface with GPIO pins w/ verilog	Evan	3/X/24
Add pic to the team website	Baoshan	3/5/24
Add bios to the team website	Evan, Baoshan	3/5/24
Get through the design portion introduction and run some simulations. Create a custom module. Start with a MUX.	Mitchell	3/5/24

Advisor Meeting Summary

Provide a concise summary of the contents and progress made during the advisor meeting.