EE/CprE/SE 491 WEEKLY REPORT 3

# Digital ASIC Fabrication

February 14, 2024 – February 20, 2024

**Group Number:** SDDec24-12

**Faculty Advisor & Client:** Henry Duwe

**Team Members:** Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

## Summary

This week, we all continued working through the steps on the ISU Chip Fab Documentation page. We made progress with accessing the lab environment and tools locally and are starting to experiment with adding simple modules to the example project directory. After creating custom modules within the project, we got through the simulation successfully. Overall, we are still getting familiar with the project layout, dependencies, and toolflow. We have run into a few issues using the tools and example Caravel project, but we got help from the graduate students.

## Past Week Accomplishments

Please describe/summarize what was done, by whom, when, and collectively as a group. This should be about a paragraph or two in length. Bulleted points are acceptable as well. Please keep only your technical details related to your project. Figures, schematics, flow diagrams, pseudocode, and project-related results are acceptable, but please ensure they are legible (clear enough to read) and explain. If researching a topic, please add details about what was learned and its relevance to the project. If two or more people worked on a single task, distinguish how each member contributed. Specific details relating to the assistance provided to other members may be included here. Do not include classwork, such as individual reflection assignments and group meetings, as part of your duties.
We continue to work on tool setup and familiarize ourselves with the toolflow and project. We are modifying the existing design files and adding our own to simulate.

- **Mitchell:** I was able to access lab tools from my personal computer. I was able to access the makefile and edit the script. I could access tools but ran into an error when running the make setup command. This issue should be resolved, but I haven't had time to test it yet.
- **Evan:** I worked on refreshing my knowledge of verilog/ learning things. I'm also in the midst of writing a few programs to hopefully simulate with the tool chain. Otherwise my time was more constricted this week. Also worked on understanding the process, understanding hardening, etc.
- **Baoshan:** I studied the workflow of Caravel projects. Additionally, I revisited the use of Verilog in simulation tools. This involves brushing up on Verilog syntax and simulation methods. Overall, it prepared me to contribute effectively to the project.
- **Katie:** I successfully ran through the example GL simulation after a little bit of troubleshooting. I also created a new simple nor gate module and testbench in Verilog

and added it to the project. I successfully simulated it through the toolflow and viewed the waveforms in GTKWave.

## Pending Issues

If applicable: Were there any unexpected complications? Please elaborate.

- **Mitchell:** Ran into an error where I was exiting the toolchain before using the make setup, which was causing variables to be undefined. This was discussed with Jake and should be resolved now. I am going to test this and if it works, continue working through wiki.
- **Evan:** still working on conceptualizing hardening and getting it to work for my native verilog projects. Although calling them projects is a bit generous.
- **Baoshan:** I've forgotten a lot of basic structures and behaviors related to HDL, such as gates and if-else statements, although I'm quite familiar with them in practice.
- **Katie:** I initially had issues with GL simulation, but I got it working after getting help from Gregory and Jake. Updating one variable in an include file made things work. I did have a few questions about hardening. After adding and synthesizing a new module to the project, what does the hardening process look like? Do you harden the overall project, or just the new module?

## Individual Contributions

| Name | Contributions | Weekly Hrs | Total Hrs |
|---|---|---|---|
| Mitchell | Accessed tools and cloned the Caravel project. Edited files and attempted to run the make setup command but ran into errors. Met with Jake to get help to continue through the wiki. | 5 | 11 |
| Evan | Simulated/attempted to harden on natively developed verilog program. Ran into bugs but I believe they were due to user error. Will further attempt/clear things up when I have more free time. | 3 | 4 |
| Baoshan | It took some time to become familiar with the DHL language, review the knowledge in previous courses, and practice simple simulations of logic circuits to obtain waveforms. | 4 | 10 |
| Katie | Ran GL simulation, added a new module to Caravel project, ran synthesis, tried hardening | 4 | 13 |

- Comments and extended discussion (Optional) Feel free to discuss non-technical issues related to your project.

## Plans for the Upcoming Week

Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.

| Action Item | Person in Charge | Expected Date |
|---|---|---|
| Create Lightning Talk slides, prepare to present | Everyone | 2/27/24 |
| Add pics to the team website | Mitchell, Baoshan | 2/27/24 |
| Attempt to view waveforms and do the example hardening | Mitchell | 2/27/24 |
| Get through the Caravel section of the wiki and attempt to go into the design portion. | Mitchell | 2/27/24 |
| Add bios to the team website | Everyone | 2/27/24 |
| Harden new module and complete gate-level simulation | Katie, Evan | 2/27/24 |

## Advisor Meeting Summary

- Begin thinking about the design aspect of the project
    - Sketch out design decomposition - overall interface and interconnections between wishbone bus, GPIO pins, I/O pins
    - Do research on the interface - look at the Verilog source files and Caravel documentation
- Work on hardening new modules
    - Want to harden each individual module before placing them into the project wrapper
- Scheduled additional meeting time for team members and with Jake as needed
    - Thursdays at 2pm