EE/CprE/SE 491 WEEKLY REPORT 2

Digital ASIC Fabrication

February 7, 2024 – February 13, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

We continued to develop our project summary and users. Our first draft description is below. This will continue to get updated throughout the semester as needed.

Project Description Draft:
Our Digital ASIC Fabrication project aims to build and silicon-prove a chip framework that will support a continuous cycle of chip designs, or “tape outs,” ready for fabrication. The project’s overall goal is to give interested students experience in chip design and fabrication. The framework we design will provide space for multiple small projects and the ability to run each independently. The project modules will be created by a co-curricular team of students ranging from freshmen to seniors. By breaking the design process into smaller, less complex subprojects, students will be able to complete modules within a semester. Each module will be fabricated and synthesized as a hard macro that can be used in our framework.

The chip framework will integrate the modules into a unified ASIC by connecting each module to the chip’s GPIOs and management wrapper, or microcontroller. All of the chip’s resources will be multiplexed between the different projects, depending on which is active at the time. The design process will involve creating a chip layout and fully-functional management core, as well as configuration scripting, Verilog coding, and C programming. The users of our project will be the students designing the modules and participating in the ISU Chip Fab Co-Curricular team. They will be familiar with the project’s purpose, setup, and tools. Once completed, the chip framework will allow the students to have their designs fully implemented and synthesized.

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Past Week Accomplishments

We continued working on tool setup and familiarizing ourselves with the toolflow. We also refined our project description and users.

- **Mitchell:** I went through the new member documentation more in-depth and was able to set up my SSH to be able to access the git repository. I worked to get my photo on the team website.
- **Evan:** This week I familiarized myself with the toolchain, along with getting an environment setup on my Z drive. To accompany this, I will finish setting up the local tools that are required (waveform viewer, etc).
- **Baoshan:** I reorganized the tools used for circuit design and physical layout. Including ModelSim, Cadence, etc.
- **Katie:** I added our last report to the website and continued working through the project setup guide. I downloaded the relevant tools on my local computer and was able to harden and view the example project in KLayout. I also drafted a description of our project and its users, which we included in the Summary.

Pending Issues

If applicable: Were there any unexpected complications? Please elaborate.

- **Mitchell:** While working on the team website, are bios about ourselves something that needs to be added? This could be discussed during the team meeting with our advisor and on our discord. I did not work hard to schedule another meeting with the group. This is something we are going to have to start doing to make real progress as a team.
- **Evan:** I need to learn or charitably ‘reacquaint’ myself with verilog, run through the process of hardening on my own verilog. I need to finish profile on our team website, and additionally make more progress on installing localized versions of layout, et al.
- **Baoshan:** We should know what type of chip we are making. In this way can we obtain more effective information in future exercises. For example, what kind of logic should be included in each small step when writing Verilog code.
- **Katie:** What should we look for after opening up a hardened design in KLayout? What are the recommended hardening config settings? These questions were discussed in our advisor meeting.

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Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Updated website, got SSH setup, continued reading through “New Member” section of chip fab	3	6
Evan	Updated website, got tool chain and env setup, hopefully grasped more of an idea of where we go from here. Completed tutorial through example hardening section.		4
Baoshan	Strengthen processes, Familiarity with design and simulation tools.	3	6
Katie	Updated website, tool setup, hardened example project, project description	4	9

Plans for the Upcoming Week

Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.

Action Item	Person in Charge	Expected Date
Create a new Verilog module and run through synthesizing and hardening steps using the toolflow. Experiment with hardening configurations in KLayout.	Katie	2/20/24
Get access and use tools in the lab. If I get comfortable try and do what Katie is doing as well. Go step by step through the design website to get a deeper understanding of the project.	Mitchell	2/20/24
Write novel verilog code. Attempt to harden it. Update website, get local tools installed.	Evan	2/20/24
Familiarity with design and simulation tool processes. And read about verification of design and simulation.	Baoshan	2/20/24
Update pics and bios on website	Everyone	2/20/24

Advisor Meeting Summary

We discussed our accomplishments listed above. We discussed as a team what each member did for the week and our thoughts on the project. We discussed with the grad students how they would recommend we get up to speed on how to use the tools in the lab and how we should prepare to start creating our design. Getting our modules running on the toolchain is a baseline for what we should accomplish next week.