Digital ASIC Fabrication

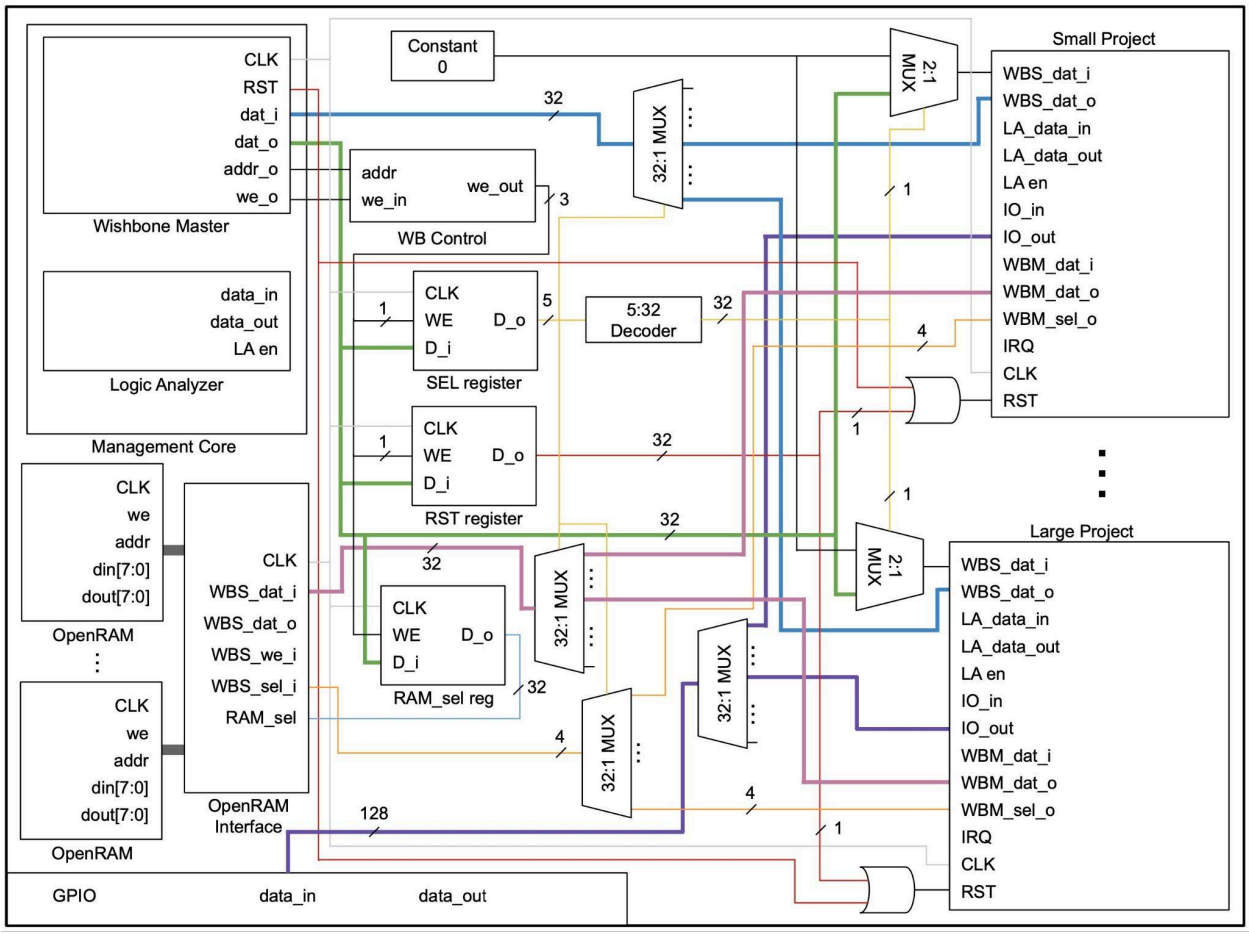
April 9, 2024 – April 16, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary



EE/CprE/SE 491 WEEKLY REPORT 10

Past Week Accomplishments

- **Mitchell:** Started Verilog for 32:1 MUX, Worked on the complete design document
- **Evan:**
- **Baoshan:** Successfully compile 5 to 32 decoder Verilog files and testbench files. After doing simulation I get a waveform.
- **Katie:** I updated the schematic to reflect what we talked about last week. I created a wishbone_control module and testbench, and it passes RTL simulation and hardening. I also successfully(?) hardened the user_project_wrapper for the OpenRAM and adder tutorials.

Pending Issues

- **Mitchell:** N/A
- **Evan:** Weird issues with implementing openRAM in the tutorial module. This could be due to it not being at the top level? Recall our project calls for openram to be in the same level as the implemented module.
- **Baoshan:** Nothing went wrong with what I did this week.
- **Katie:** Do we need to run GL simulation on all subcomponents? Reason behind inconsistent hardening results of same project repos?

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Verilog for MUX and design document work	2	40
Evan	This week I did some research into openram, and getting it to successfully harden. I was vaguely unsuccessful due to previously documented errors:	~4-6	41
Baoshan	Complete the design of the decoder (part of the schematic)	5	38
Katie	Updated schematic, wishbone control module, hardening user_project_wrapper	5	48

Plans for the Upcoming Week

Action Item	Person in Charge	Expected Date
Final presentation!!!!	Everyone	4/23/24
	Evan	5/x/24
	Katie	4/x/24
	Mitchell	4/x/24
Commit decoder files	Baoshan	4/24/24

Advisor Meeting Summary