Digital ASIC Fabrication

January 23, 2024 – February 6, 2024

Group Number: SDDec24-12

Faculty Advisor & Client: Henry Duwe

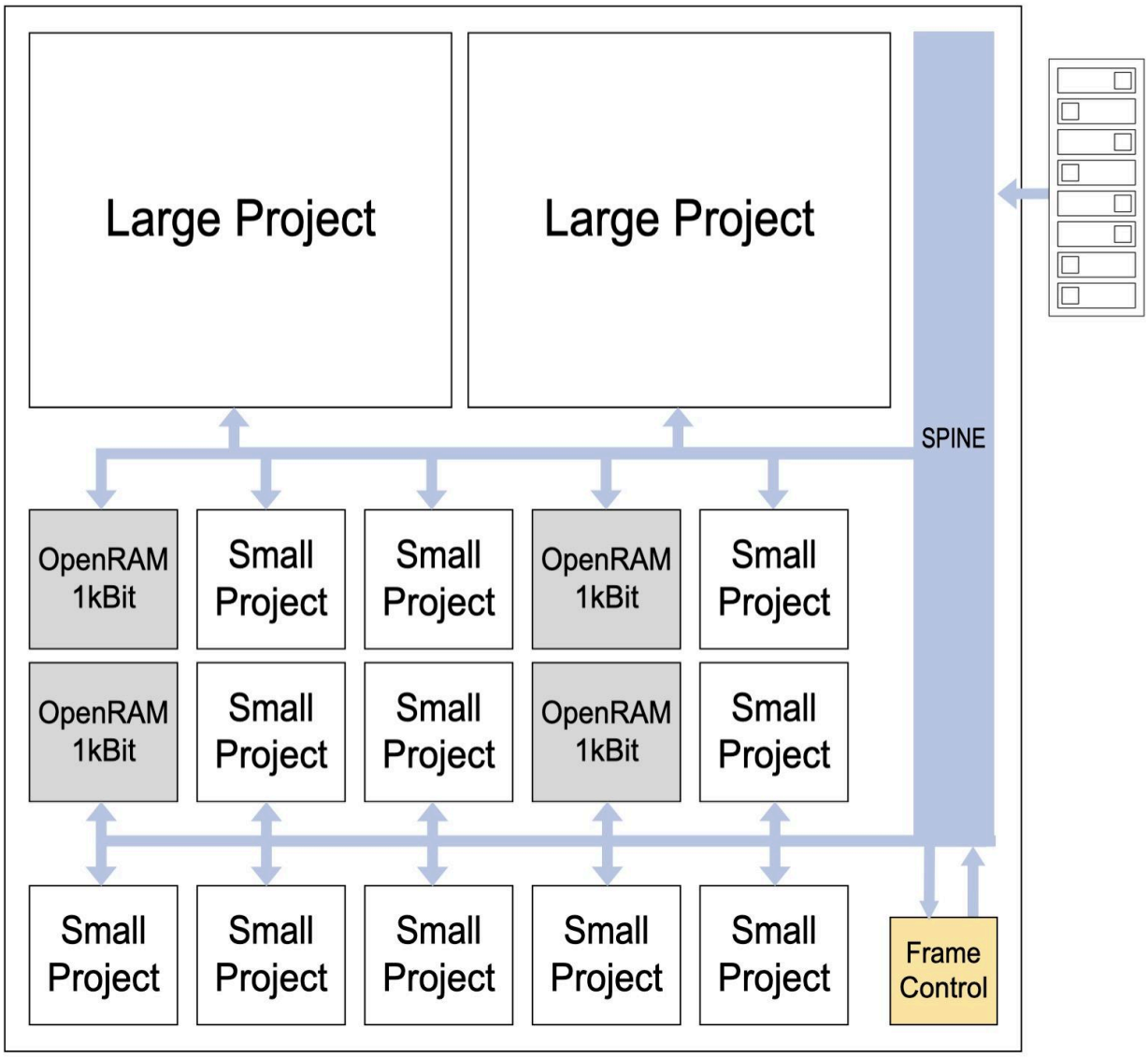
Team Members: Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Summary

This week, we primarily focused on organization. To start, we had our initial meeting with Dr. Duwe and the Master's students that we will be working with on 1/30/24. We have been given tons of documentation on how to use the different tools and links that will help us learn about our project. We were introduced conceptually to the weekly reporting system. Finally, we were granted access to the project website, Teams group, and various resources we will be working with for the rest of this year. Overall, we took the first step on the road to finishing our senior project.

During our meetings with Dr. Duwe, we were given a brief overview of what the goal for our project was. We will be building the framework in order for future students to be able to use and gain experience in fabrication that they would not gain otherwise. Our end goal is to create a chip framework that can hold a set amount of smaller projects that can run independently from each other. The figure below shows a general idea of what the end product will be. The users of our project will be future students participating in the ISU Chip Fab Co-Curricular. These students will range from freshmen to seniors, and they will already have knowledge about the platform, tools, and purpose of the project.

The upcoming build deadline is June 3. If we are able to have our design finished and ordered by then, we would be able to get the physical chip back in the Fall. We do not necessarily have to meet this deadline, but doing so would put us in a great position to go beyond the goal of this project in the Fall 2024 semester.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Past Week Accomplishments

This week was the introduction to the environment and group that we will be working with, so progress was mainly set up. Mainly, we all worked to gain access to the lab and server, looked into material about our project, and finally introduced ourselves to our group, Dr. Duwe, and the Master's students that will be assisting us this semester.

- **Mitchell:** I spent time setting up a Google Drive for our team and putting in and formatting the report page template. I also spent some time updating our weekly report. I gained key access to Durham and the 310 lab room and began reading about previous groups' progress and projects.
- **Evan:** Once we established how to access the server, work was done on updating his user profile, contributing to the report, and altogether just diving into the technology and tasks required for this senior project.
- **Baoshan:** I have looked up some information on the Internet regarding chip design and layout. I have a rough understanding of the process and the tools I need to use, as well as how to program and test.
- **Katie:** I added our project abstract and updated our group members on the team website and requested key access to the Durham building and lab. I was able to clone the Caravel template into our team's GitLab repo, and I sshed onto the lab computer. I started running through the build steps and setting up the different tools we will be using.

Pending Issues

- N/A. This was an introductory week, where we were expected to familiarize ourselves with the technology and environment. We have not run into any issues yet.

Individual Contributions

Name	Contributions	Weekly Hrs	Total Hrs
Mitchell	Report, Key Access, Reading	3	3
Evan	Website, technology, report, getting keys	4	4
Baoshan	Read, verify information, streamline processes.	3	3
Katie	Key access, website, GitLab repo, tool setup	5	5

Plans for the Upcoming Week

- **Mitchell:** I plan to spend considerable time learning about the current projects and how to use the lab equipment. Meeting as a team and discussing what we can do would be beneficial before our next meeting. Try to SSH and run the design to view waveforms. Gain an understanding of what the signals mean.
- **Evan:** I plan to delve into the system which runs our current chipset, try some basic development, and/or simply look more into what is expected of our group.
- **Baoshan:** I plan to establish an IC design process so that we can have a clearer understanding of the progress of our work and identify the software needed for each specific step (such as RTL code or simulation).
- **Katie:** I plan to continue following the tool tutorials and run sample hardening. I want to try creating my own module and going through the same steps as the guide. I also plan to further set up our GitLab repo, and read through documentation from previous groups.

Advisor Meeting Summary

During our meeting with Dr. Duwe on 2/6/24, we reviewed the goal of our project and went into more detail about our project's functionality. We talked about the general timeline of the project and tasks to work on for next week's meeting.

- Overall Goals:
    - Have consistent chips "taped out" for fabrication and brought up by the ISU Chip Fab Co-Curricular team
    - Have a chip subdivided into different, smaller modules or projects created by a student or pair of students
    - Give students fabrication experience they wouldn't get in coursework
- Specific Project Goals:
    - Create the framework for the chip that connects the submodules
    - Develop design for framework, as well as modules
- Notes:
    - Frame hooks different projects to each other, GPIOs, management wrapper, microcontroller
    - Submodules will be created by individual or pairs of students; they will not be overly complex
    - Submodules can be fabricated and synthesized on their own; they will be macros that can be used in other designs without any modification
    - Project will involve working with Verilog, config files, and C programs for testing with the microcontroller
- TODO:
    - Write a 2 paragraph project summary detailing what our project is about and who our users are
    - Begin a list of specific requirements for our project