# Digital ASIC Fabrication: Design – Part 2

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**Client & Faculty Advisor** 

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### **Project Overview**

#### **Problem Statement**

 Undergraduate students rarely get the opportunity to create a custom digital ASIC (Application Specific Integrated Circuit) and gain experience with chip fabrication.

#### **Project Goals**

- Our project aims to give interested students experience in chip design and fabrication.
- We plan to build a chip framework that will hold small ASIC projects created by students in a co-curricular team.
- The chip framework will allow the students to have their designs fully implemented and synthesized.

# Detailed Design

- Our framework goes into the user project wrapper
- Framework interacts with the management area and user projects
- Interfaces directly with Wishbone bus, logic analyzer, GPIOs
- Management area configured through software





CLK - System clock

**GPIO** - General-Purpose Input/Output

**IO** - Input/Output; data transfer to or from the chip

**IRQ** - Interrupt Request Signal

LA - Logic Analyzer

RST - Reset

**WB** - Wishbone Bus

**WBS** - Wishbone Slave

WE - Write enable

### Functionality

- Users will design independent ASIC projects that will be used as macros in our framework
- Multiple projects can be placed in the framework at once
- Each project can be run independently and access the management core



## **Technology Considerations**

- Mainly using open-source tools and project framework
- Pros:
  - Regular updates
  - Cost-effective
- Cons:
  - Limited support
  - Learning curve
  - Limited compatibility

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#### **Concerns and Development**

#### Areas of Concern

- Will current level of complexity support all possible projects going forward?
- With current level of complexity, will all expected modules fit in die area?

#### **Areas of Development**

- Power optimization
  - Clock gating
- Preserving inactive project state

#### Conclusion

- Current design composition is our base design going forward
- Will incorporate more functionality as needed
- Plan to integrate OpenRAM components
- Refine design and constraints as we implement submodules