Digital ASIC Fabrication:

Design - Part 1

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Project Overview

Problem Statement

- Undergraduate students rarely get the opportunity to create a custom digital ASIC (Application Specific Integrated Circuit) and gain experience with chip fabrication.

Project Goals

- Our project aims to give interested students experience in chip design and fabrication.
- We plan to build a chip framework that will hold small ASIC projects created by students in a co-curricular team.
- The chip framework will allow the students to have their designs fully implemented and synthesized.

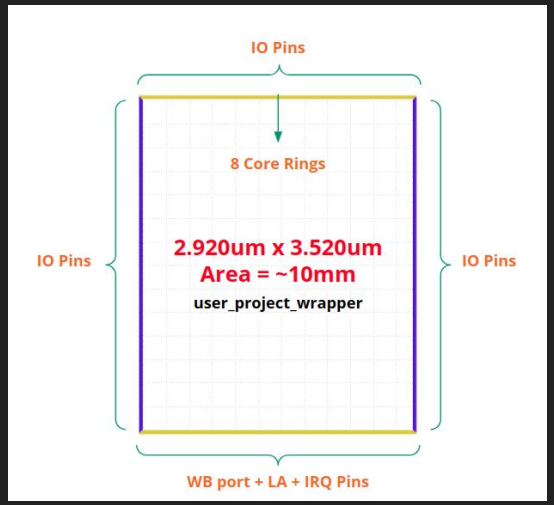
Project Ideation

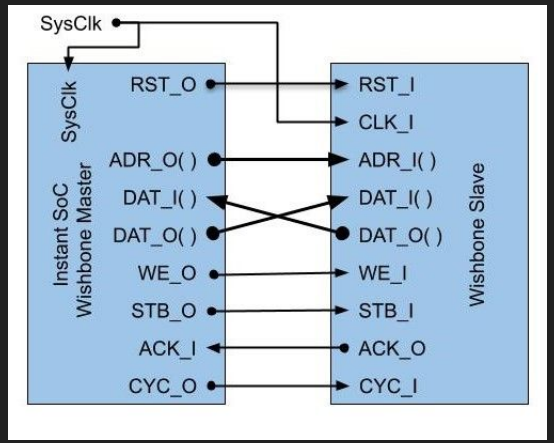
Research

- Caravel project framework
- Provided components
  - Management Core, Wishbone Bus
- Synthesize and harden example projects
  - Existing ports, configurations

Design Decisions

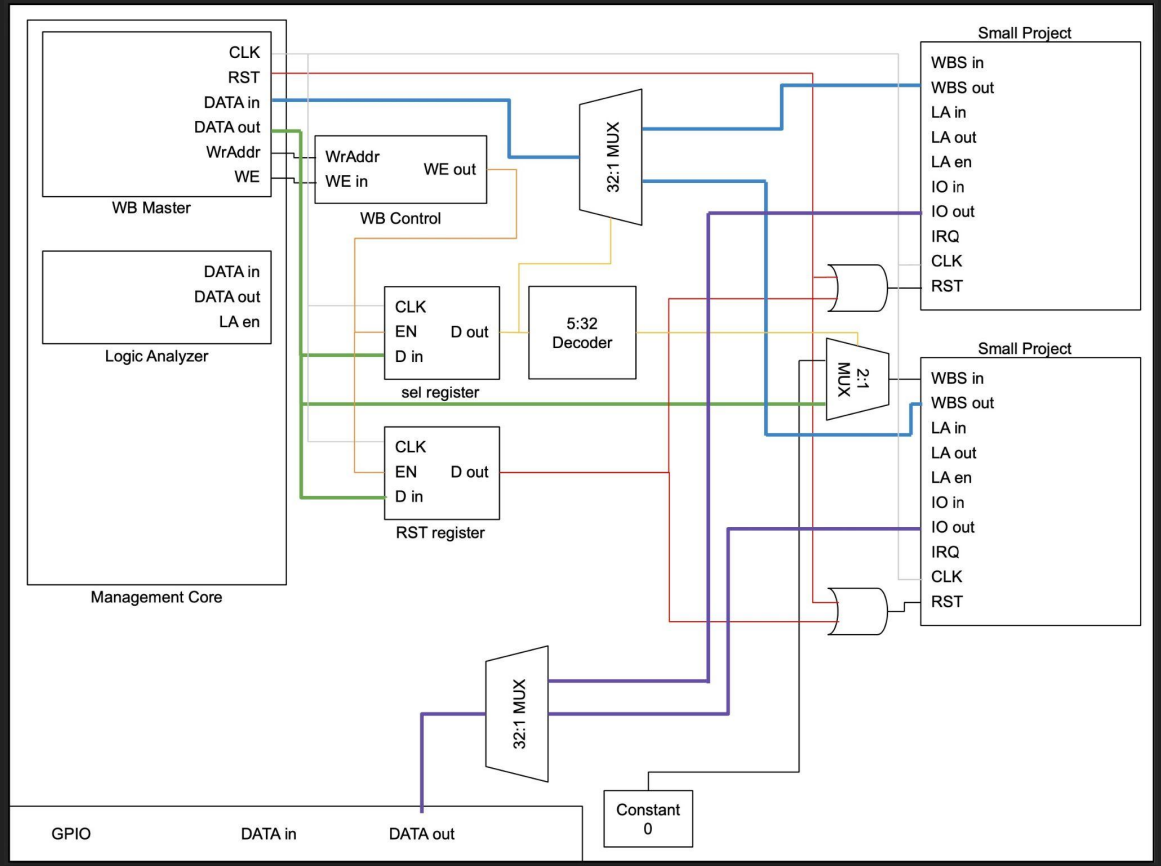
- How to connect projects?
- How to control framework
  - Physical switches vs. software





Proposed Design

- High-level composition
- Connect management core to user projects
- Multiplex resources based on active project
- Individual project reset
- Dedicated control registers and memory space



Market Research

- Several large, established ASIC manufacturers
- Different focus areas - electronics, automotive, etc.

Takeaways

- Importance of design optimization - power, area
- Testing and validation process

Opportunities

- Reduced cost
  - Custom ASICs can cost $1M
- Addressing specific needs/markets
  - General-purpose ASICs can’t provide specific functionality as efficiently

Next Steps

- Integrate OpenRAM components into framework
- Harden example projects
- Consolidate hardening data - sizes, ports, layout, frequencies
- Refine design composition