

Digital ASIC Fabrication:
Project Plan

Team 12

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Project Overview

Problem Statement

- Undergraduate students rarely get the opportunity to create a custom digital ASIC (Application Specific Integrated Circuit) and gain experience with chip fabrication.

Project Goals

- Our project aims to give interested students experience in chip design and fabrication.
- We plan to build a chip framework that will hold small ASIC projects created by students in a co-curricular team.
- The chip framework will allow the students to have their designs fully implemented and synthesized.

Project Management Style

Waterfall Style

- We will be using a waterfall management style. Our project has set goals that are required before we can continue moving forward to the next step. Additionally, We have a set outcome of what our project should look like and how it should function. We do not plan on changing the functionality or scope of our project too much during our development.

Task Decomposition



Milestones

Task	Jan				Feb				March				April				May				June				July				Aug				Sept				Oct				Nov				Dec							
	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4								
Tool Setup																																																				
Simulate and harden sample Caravel project																																																				
Get familiar with toolflow, GTKWave, KLayout																																																				
Design Decomposition																																																				
Research wrapper components																																																				
Plan out framework schematic																																																				
Create Modules																																																				
Implement modules in Verilog																																																				
Test and harden each module																																																				
Integrate Modules																																																				
Verify individual modules meet requirements																																																				
Add modules to project wrapper																																																				
Test Overall Design																																																				
Test projects inside of wrapper framework																																																				
Verify RTL simulations and hardening pass																																																				
Verify GL simulations pass																																																				
Submit Design to eFabless																																																				
Create eFabless repository and project																																																				
Submit the design by the June 3 deadline																																																				
Bring-Up and Physical Testing																																																				
Document detailed bring-up plan																																																				
Test physical chip																																																				

Risks and Mitigation

Risks

- Not meeting June 3rd deadline
- Physical functionality is not as intended

Mitigation

- Plan each step out in detail to stay on track and meet deadlines
- Thoroughly test each component to give us the greatest chance for success.

Conclusion

We have a set plan and using the waterfall style of project management we should be able to follow our task decomposition to complete each milestone before moving on to the next. By thinking about our risks now we should be able to avoid most setbacks. There will always be problems that arise in the future but by working together now and thinking about these problems we will hopefully avoid most setbacks.