Digital ASIC Fabrication:

User Needs and Requirements

Team 12
Mitchell Driscoll, Evan Dunn, Baoshan Liang, Katie Wolf

Project Overview

Problem Statement

- Undergraduate students rarely get the opportunity to create a custom digital ASIC (Application Specific Integrated Circuit) and gain experience with chip fabrication.

Project Goals

- Our project aims to give interested students experience in chip design and fabrication.
- We plan to build a chip framework that will hold small ASIC projects created by students in a co-curricular team.
- The chip framework will allow the students to have their designs fully implemented and synthesized.

User Needs

Undergraduate Students at Iowa State

- Need an accessible way to synthesize and fabricate their own ASIC projects because they are interested in chip fabrication and want to gain experience

Graduate Students at Iowa State

- Need a functional chip framework because they want to guide younger students in ASIC fabrication and gain experience for their future career

ECpE Professors at Iowa State

- Need a way to implement projects created by the ISU Chip Fabrication Co-curricular team because they want to help undergraduate students gain chip fabrication experience outside of class

Hardware-Based Requirements

- Framework holds 15 small projects and 2 large projects
- Management wrapper controls which project is active
- One project can be active at a time
- Chip resources can be multiplexed between all the projects
- Wishbone bus has 32-bit read/write data
- Memory uses existing OpenRAM module
- The final design will be generated in a GDS2 file
- Framework design meets eFabless requirements
- The design successfully simulates and hardens
- Code will be written in Verilog and C

User-Based Requirements

- Fully documented on the ASIC project website. Detailed description of the project that allows users to understand architecture.
- Straightforward to use with minimal help or troubleshooting.
- Sets the framework for ISU Chip Fab club.
- Framework is controlled through a makefile.

Engineering Standards

- **IEEE 1364-2005** - Verilog Hardware Description Language
- **ISO/IEC 9899:2018** – C Programming Language (C17)
- **IEEE 1481-2019** - Integrated Circuit (IC) Open Library Architecture
- **IEEE 1076.4-2000** - VITAL ASIC Modeling Specification

Conclusion

By creating our framework within the chip, we are giving more students the opportunity to gain chip fabrication experience while also being as efficient and cost effective as possible.

Throughout our design process, we will consider these requirements and standards to ensure our project meets all expectations for our users and industry professionals.