Digital ASIC Fabrication

Faculty Panel Presentation

sddec24-12
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Client & Faculty Advisor
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Project Overview

Problem

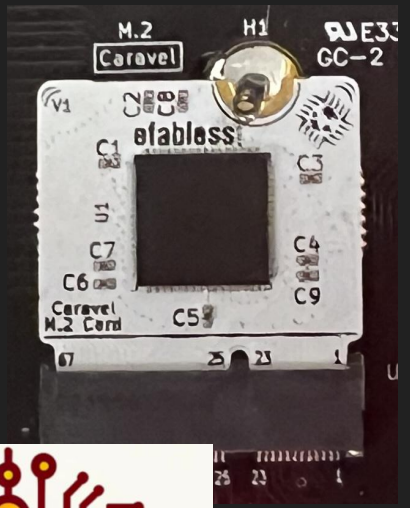
- Undergraduate students rarely design and fabricate custom ASICs

Goal

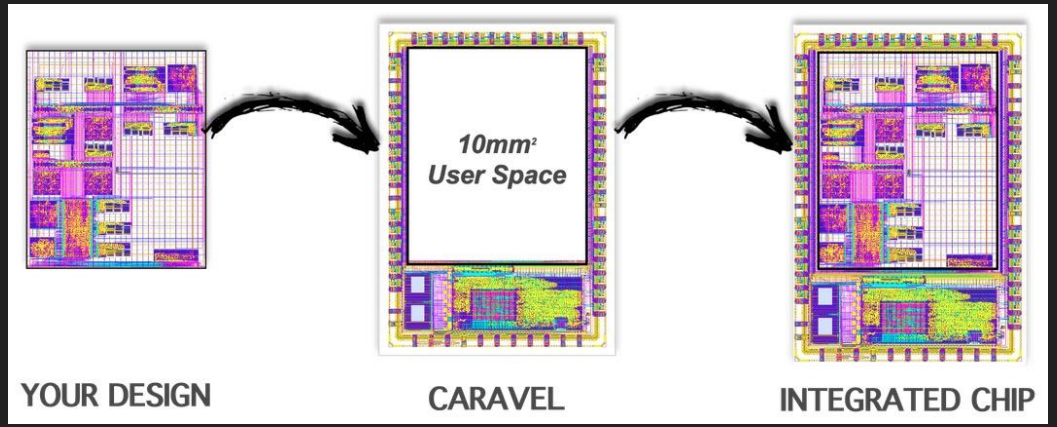
- Support co-curricular at ISU for students interested in chip fabrication

Purpose

- Chip framework for student projects
- Amortize cost of fabrication

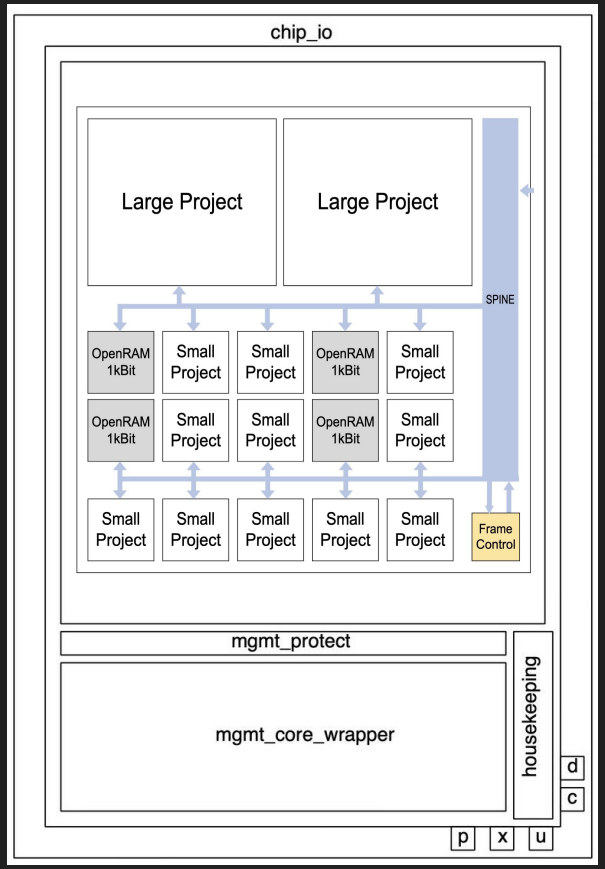


Open-Source Design



[1]

Efabless Pre-Designed Chip Harness



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Users

1.

Future Students

Fabrication opportunities

2.

Professors & Educators

Provide learning opportunities

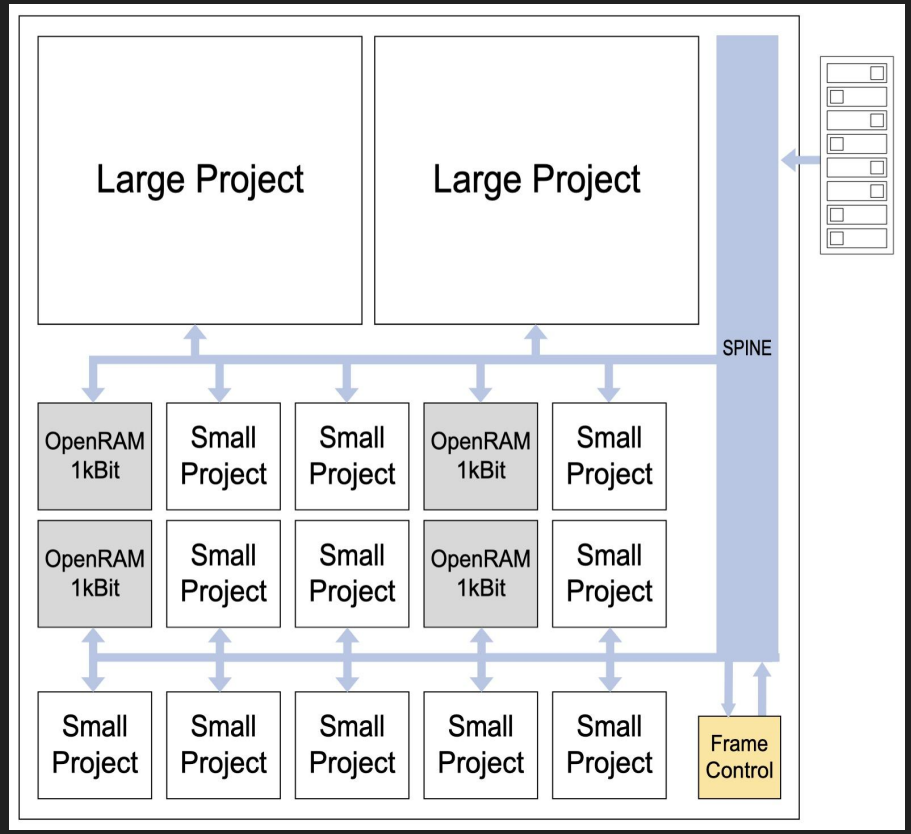
3.

Open-Source Community

Project resources and collaboration

Functional Requirements

- 15-20 total projects - large and small
- Microcontroller selects which project is active
- One project is active at a time
- Projects interface with Wishbone bus, LA pins, and IO pins
- Include external OpenRAM modules
- Design successfully passes prechecks



Non-Functional Requirements

Technical Requirements

- Use Efabless process
- Design implemented in Verilog
- Test code written in Verilog and C
- Frequency of 20 MHz

User-Based Requirements

- Full documentation and bring-up plan
- Straightforward to use with minimal help or troubleshooting
- System is modular and users can expand upon it

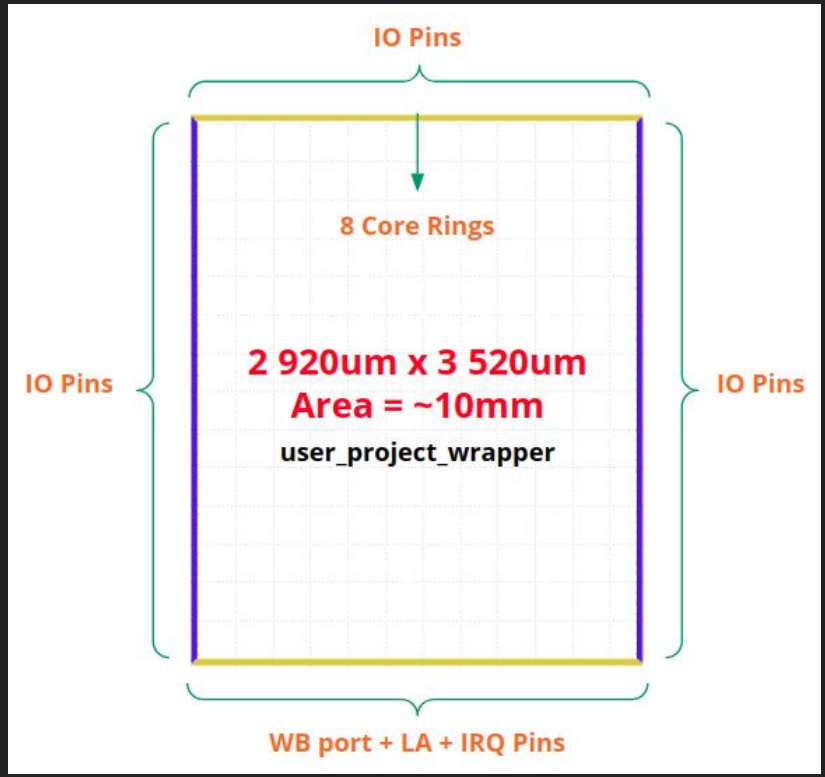
Constraints

Efabless Requirements

- 2920um x 3520um user area
- Caravel file and directory structure
- 128 LA pins
- 38 I/O pins

Additional Considerations

- OpenRAM module placed on top layer



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Market Comparison

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- Tiny Tapeout
  - Provides too-little space
  - Insufficient testing interface for development process
  - Not suitable for extracurricular requirements
- Increased space, distributed cost
- Specific needs addressed
  - Easily mapped one student/group to one project - greater feedback
- Reusable, modular design
  - Redundancy - one broken/misfabricated module doesn’t shutter project
  - Projects tested in isolation, independently structured

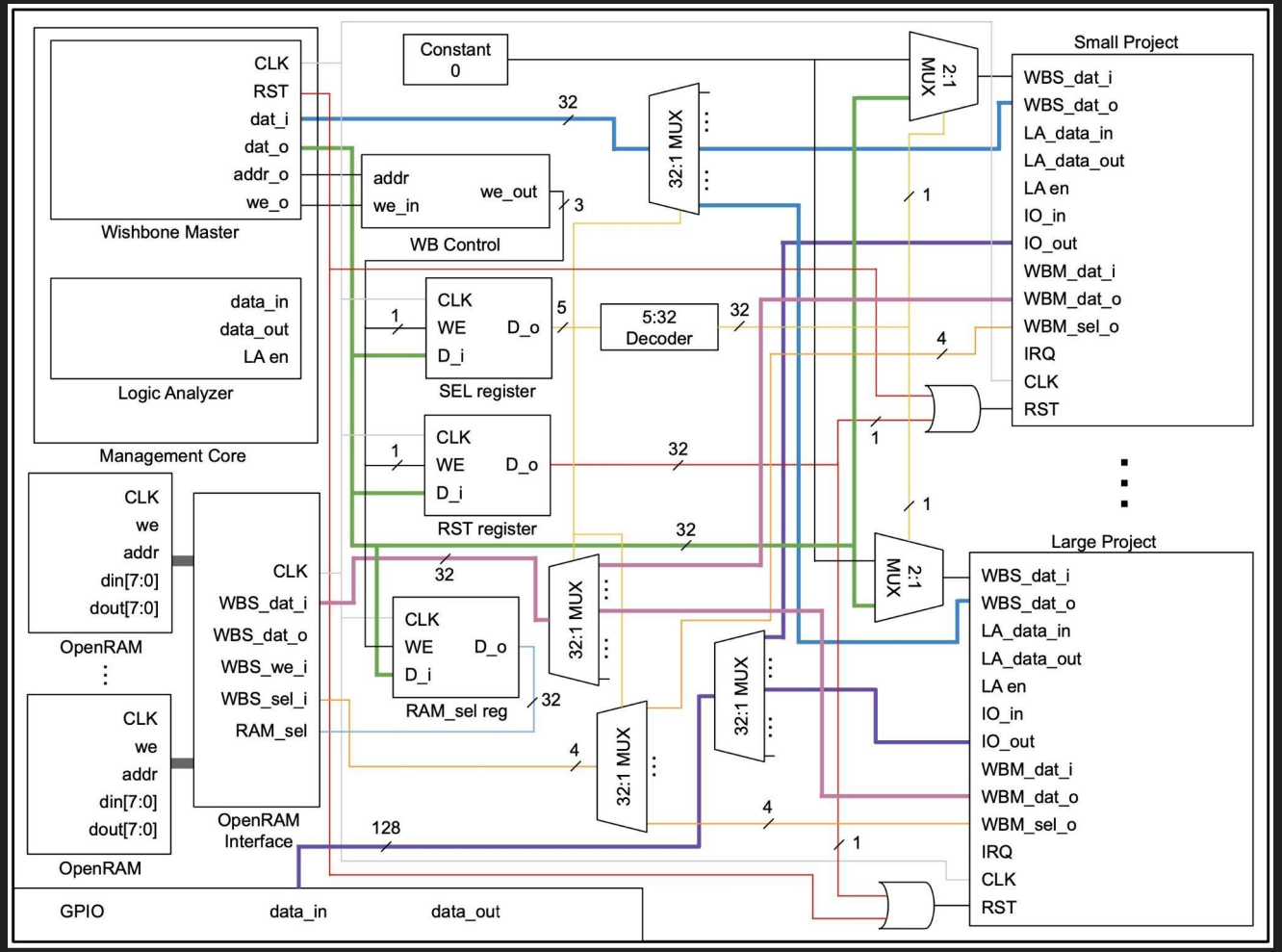
Resource & Cost Estimation

- Program – $9750
  - 4-5 month turnaround - compatible with academic year
  - Without framework: 15 projects × $9750 = $146,250 estimated sum
- Open-source software – no licensing costs
  - More long-term support
  - Can be maintained by co-curricular team
  - Forking and customization of materials

Potential Risks

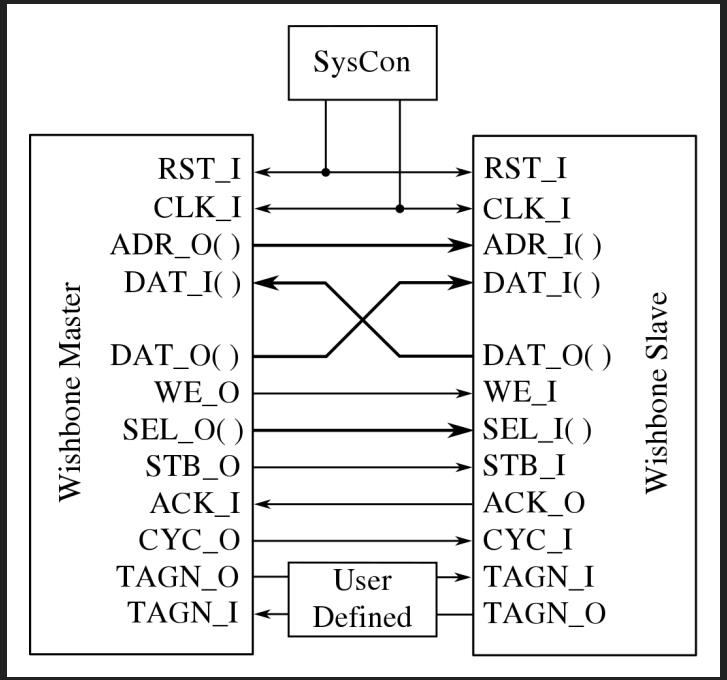
Risk	Probability
Design doesn’t pass precheck	15%
OpenRAM interface doesn’t meet timing requirements	10%
User area cannot fit spine and expected projects	10%
Error occurs during fabrication and delivery	5%

Design


Constant 0
Small Project
WBS_dat_i
WBS_dat_o
LA_data_in
LA_data_out
LA en
IO_in
IO_out
WBM_dat_i
WBM_dat_o
WBM_sel_o
IRQ
CLK
RST
2:1 MUX
32:1 MUX
CLK
RST
dat_i
dat_o
addr_o
we_o
Wishbone Master
addr
we_in
we_out
WB Control
data_in
data_out
LA en
Logic Analyzer
Management Core
CLK
WE
D_i
D_o
SEL register
5:32 Decoder
RST register
RAM_sel reg
CLK
we
addr
din[7:0]
dout[7:0]
OpenRAM
OpenRAM
CLK
WBS_dat_i
WBS_dat_o
WBS_we_i
WBS_sel_i
RAM_sel
OpenRAM Interface
Large Project
GPIO
data_in
data_out

Interfaces

- Wishbone Bus
  - Interface between microcontroller and user projects
- Logic Analyzer Probes
  - Signals driven or monitored by microcontroller
- Input/Output Ports
  - Programmable pins to send or receive data externally



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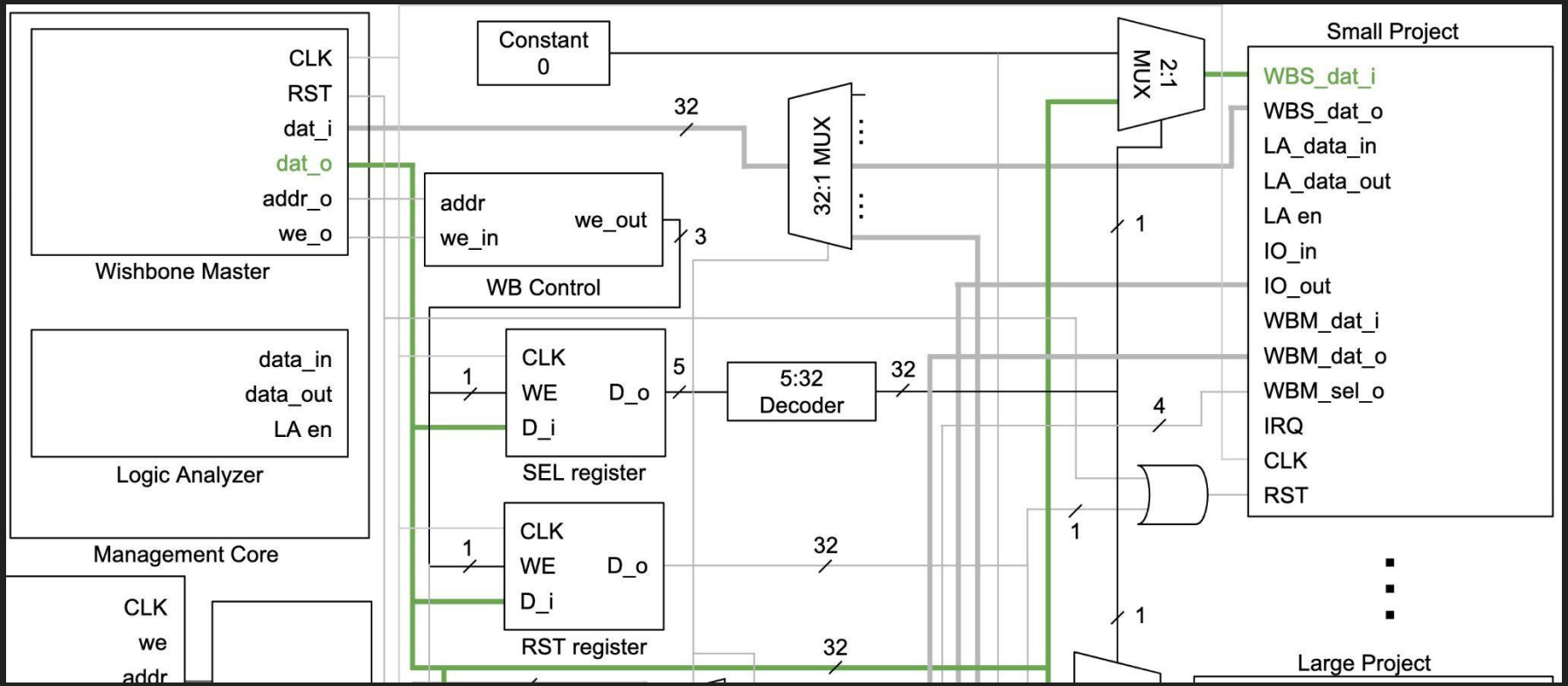
Control Registers

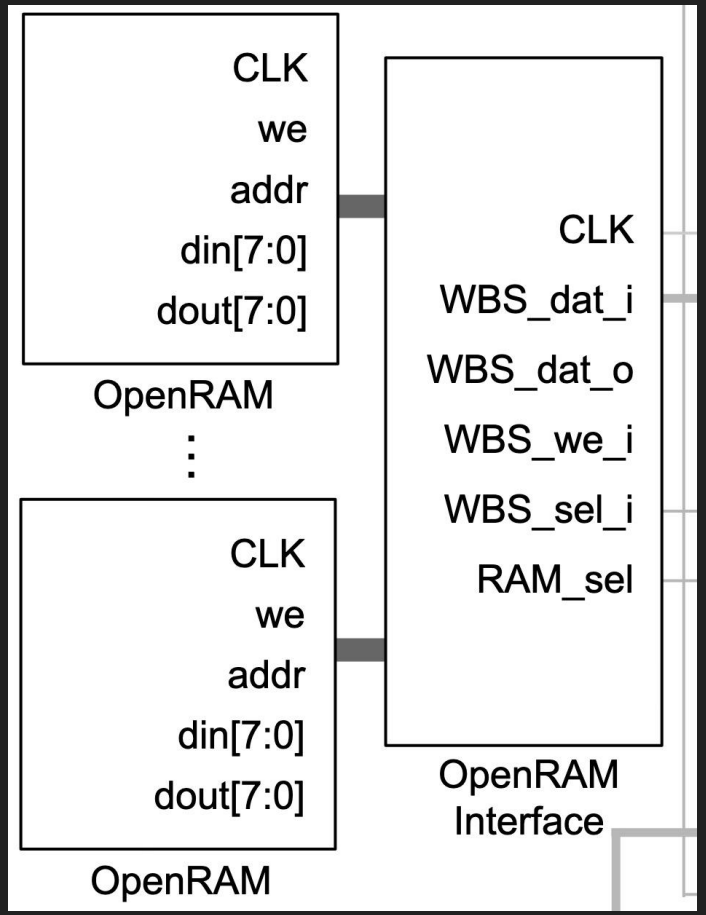


OpenRAM

- Pre-hardened module - 8-bit data
- Use 4 modules to support 32-bit data

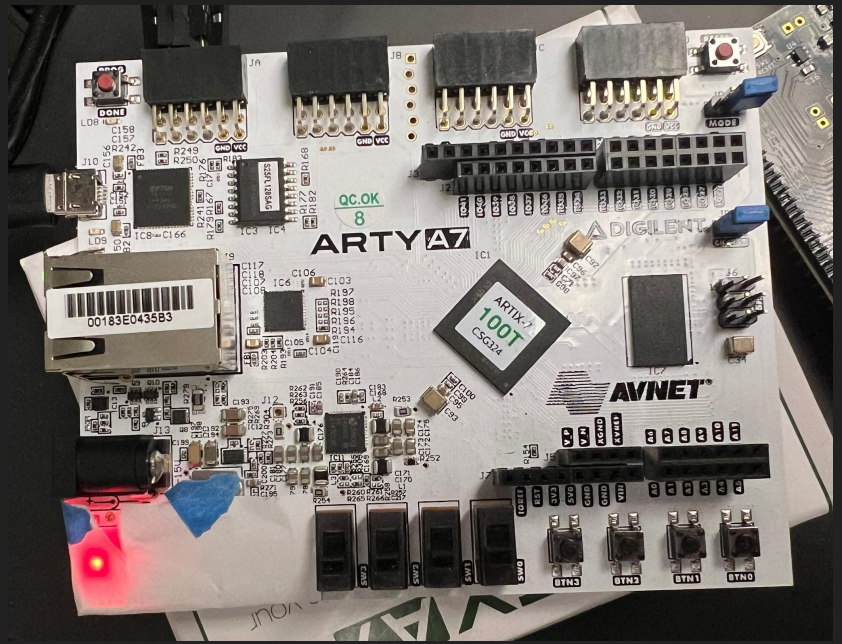
Interconnection with User Projects

- Add ports for all 4 modules
  - Straightforward
  - Add 4 sets of OpenRAM ports
- Wishbone interface
  - Add 1 set of Wishbone master ports



Tools & Technology

- **Caravel** – Chip harness
- **OpenROAD** – Synthesis toolflow
- **GTKWave** – Waveform viewer
- **KLayout** – Layout viewer
- **FPGA Board** - Pre-fabrication testing



Unit Testing

- Register Transfer Level (RTL) Simulation
- Hardening
- Gate-Level (GL) Simulation

- Modules
  - N-bit register
  - 5 to 32 decoder
  - 32 to 1 multiplexer
  - Wishbone control module
  - OpenRAM interface
  - User projects

- Test hardening user projects to find constraints

Unit Testing Results

N-bit Register Waveforms

Wishbone Control Waveforms

Hardening Results

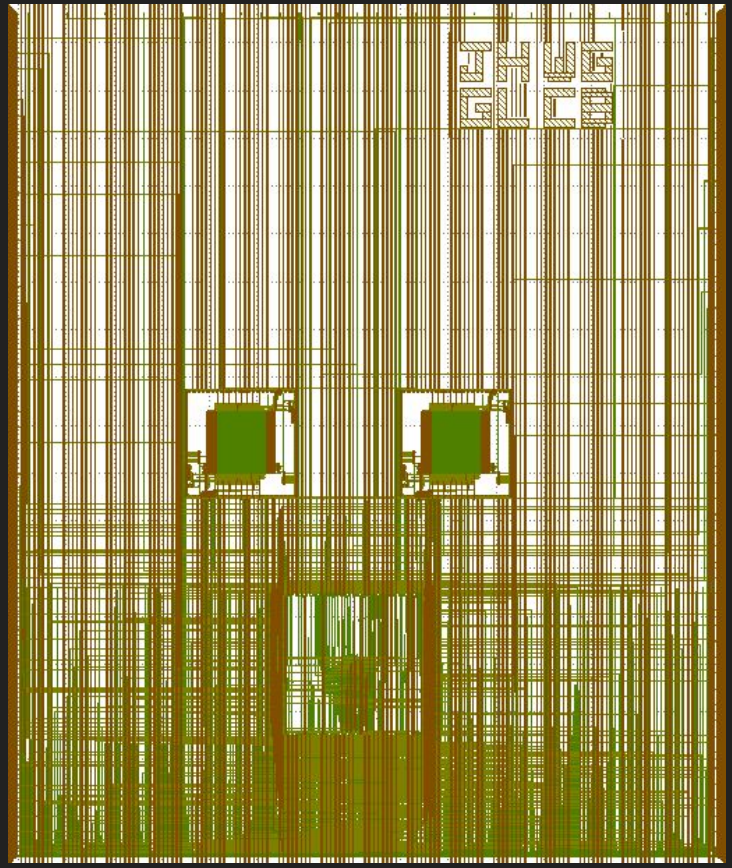
Component	Run #	Changed Settings	# Ports	CLOCK_PERIOD	CLOCK_PORT	CLOCK_NET	FP_SIZING	DIE_AREA	PL_TARGET_DENSITY	Pass? (Y/N)
adder_wrap	9	Added WB master ports	711	25	wb_clk_i	[blank]	absolute	0 0 700 700	0.55	Y
adder_wrap	10	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 501 501	0.55	N
adder_wrap	11	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 550 550	0.55	N
adder_wrap	12	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 575 575	0.55	N
adder_wrap	13	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 600 600	0.55	Y
adder_wrap	14	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 585 585	0.55	N
adder_wrap	15	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 586 586	0.55	N
adder_wrap	16	DIE_AREA	711	25	wb_clk_i	[blank]	absolute	0 0 587 587	0.55	Y

Die Area Tests

$10mm^2$ / $.587mm^2$ = 29 possible projects

Integration Testing

- Interconnections
  - Wishbone bus
  - Logic analyzer
  - IO pins
  - OpenRAM interface
- Utilize previous senior design projects



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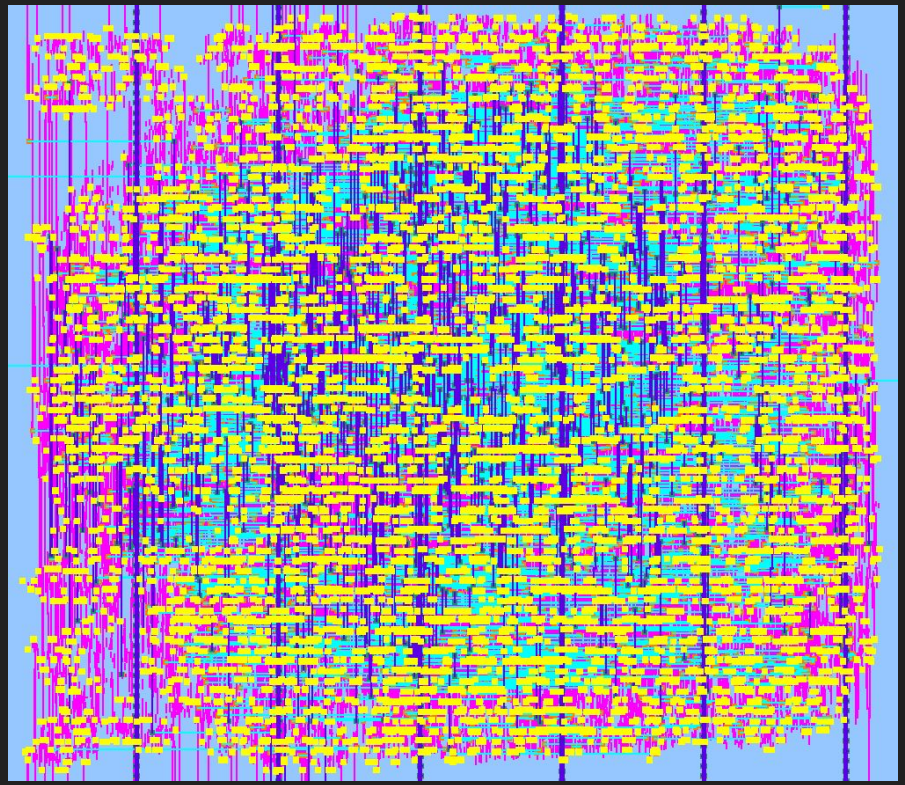
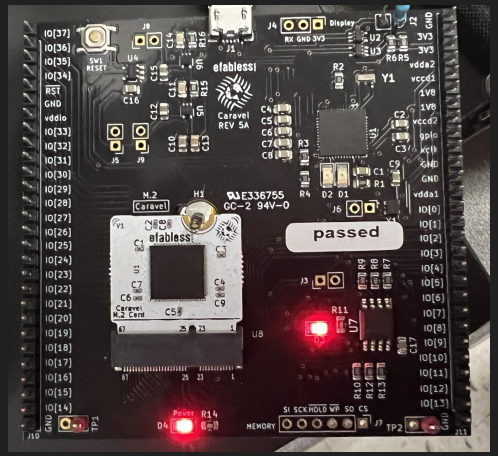
Acceptance Testing

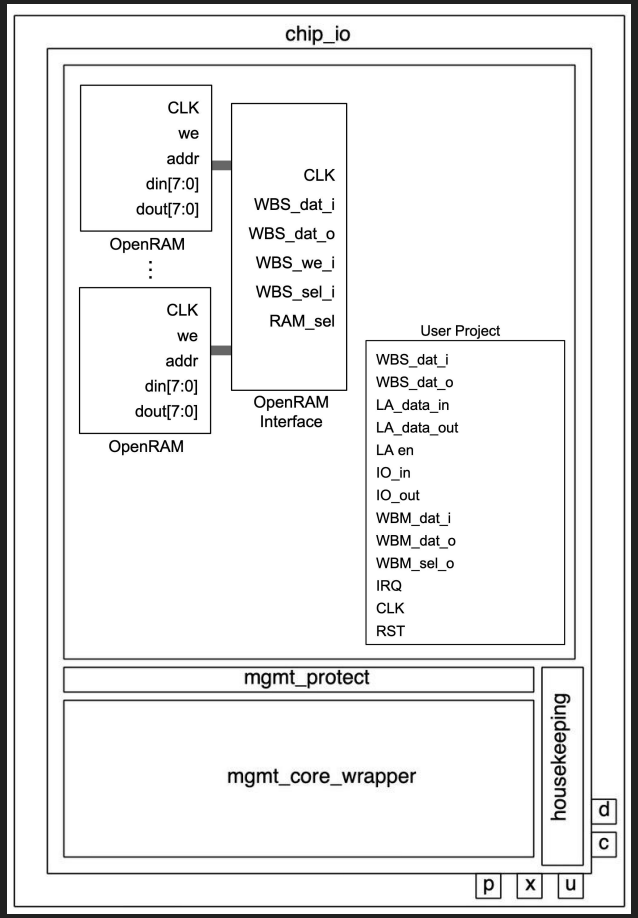
- Harden top-level design
  - Place and route
  - Optimal hardening configuration
- Caravel precheck
  - Required for Efabless submission
  - Layout Versus Schematic (LVS)
  - Design Rule Check (DRC)



Bring-Up Testing

- Physical testing on FPGA
- Future testing plan
  - Testing template with OpenRAM interface
  - Bring-up boards





Project Status

Complete	In Progress	Next Steps
Tool Setup	Module Implementation	Framework Integration
Design Decomposition	RTL Simulation	High-Level Testing
Hardening Data	Module Hardening	Framework Hardening

Project Schedule

Task	Status	Jan	Feb	March	April	May	...	Aug	Sept	Oct	Nov	Dec
Project Setup	Done											
Setup tools and workspace	Done											
Example project tutorials	Done											
Design Decomposition	Done											
Research components	Done											
Draw schematic	Done											
Create Modules	In Progress											
Implement modules	In Progress											
Test and harden each module	In Progress											
Integrate Modules												
Add modules to project wrapper												
Implement interconnections												
Test Overall Design												
Test interconnections												
Test user projects												
Submit Design to Efabless												
Bring-Up and Physical Testing												
Test on firmware												
Create bring-up plan												

Team Roles

Wishbone Interface	Top-Level Design	Place and Route
Katie	Mitchell Katie	Evan

Integration Testing	Acceptance Testing	Bring-Up Plan
Mitchell Baoshan	Evan Baoshan	Mitchell Katie

References

[1] https://efabless.com/open_shuttle_program

[2] https://caravel-harness.readthedocs.io/en/latest/

[3] https://github.com/efabless/caravel_user_project/blob/main/docs/source/index.rst

[4] https://tinytapeout.com/

[5] https://en.wikipedia.org/wiki/Wishbone_(computer_bus)

[6] https://sddec23-06.sd.ece.iastate.edu/

Thank you!

Questions?